

MODEL NAME : Maple
PCB NO : DA8000WL000 LA-B012PR01

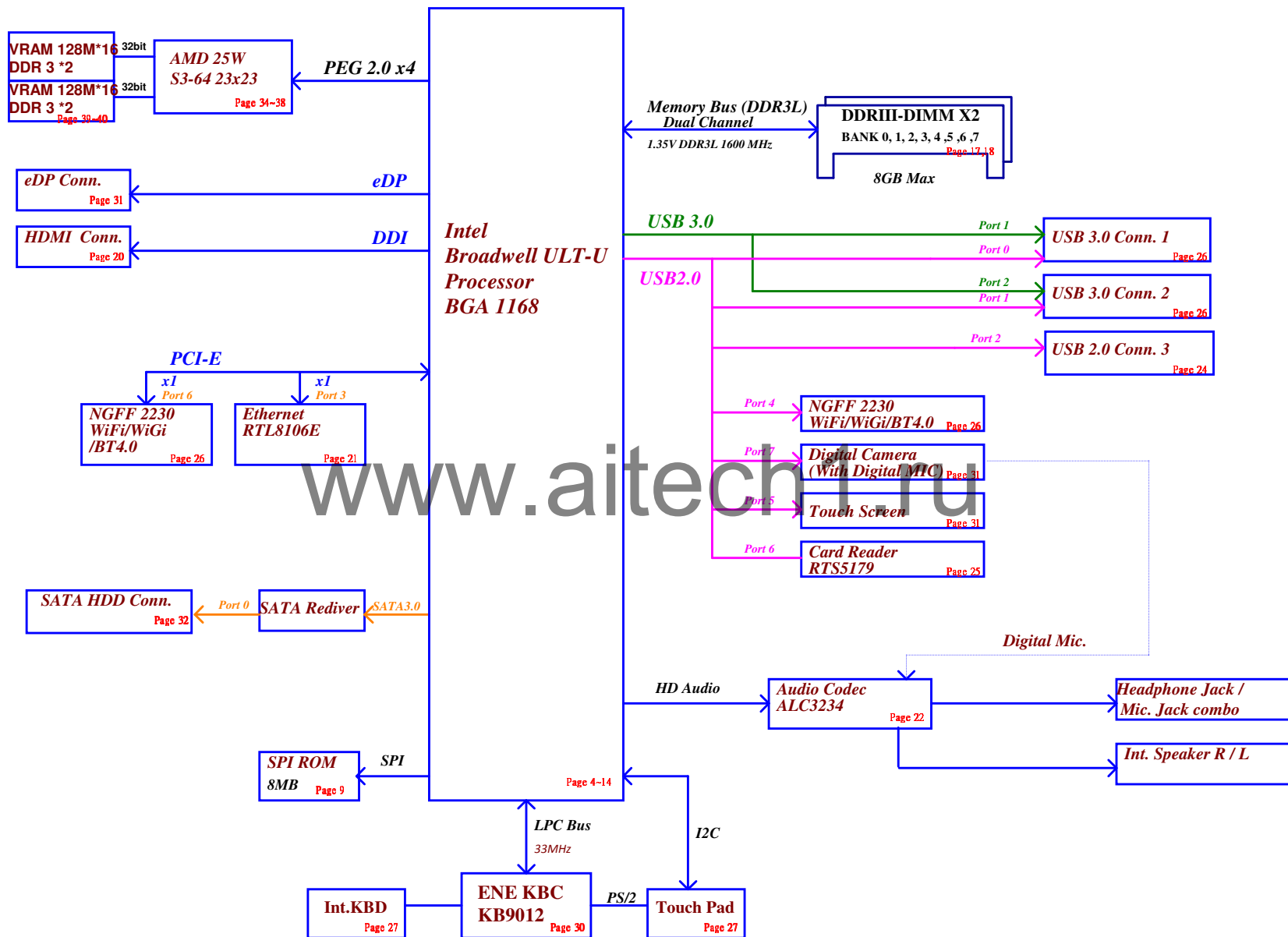
Dell / Compal Confidential

Schematic Document

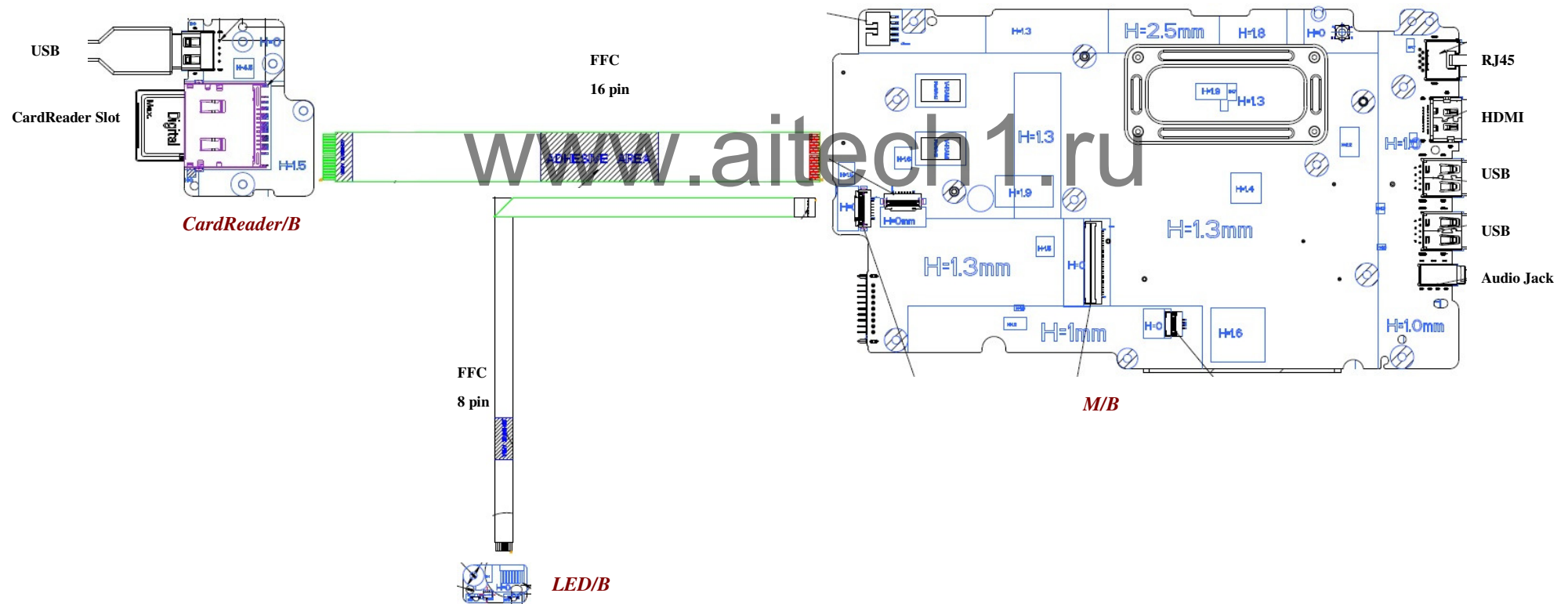
Intel Shark Bay ULT
Maple 14"/15" Value
UMA / DIS AMD 25W/S3+DDR3x4

2014-01-21 Rev: 1.0

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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

HSW BOARD ID Table

Board ID	UMA	DIS (JET)	DIS (Topaz)
0	SSI		
1		SSI	
2			SSI
3	PT		
4		PT	
5			PT
6	ST		
7		ST	
8			ST
9	1.0		
10		1.0	
11			1.0


BDW BOARD ID Table


Board ID	UMA	DIS (JET)	DIS (Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XD	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V				
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	

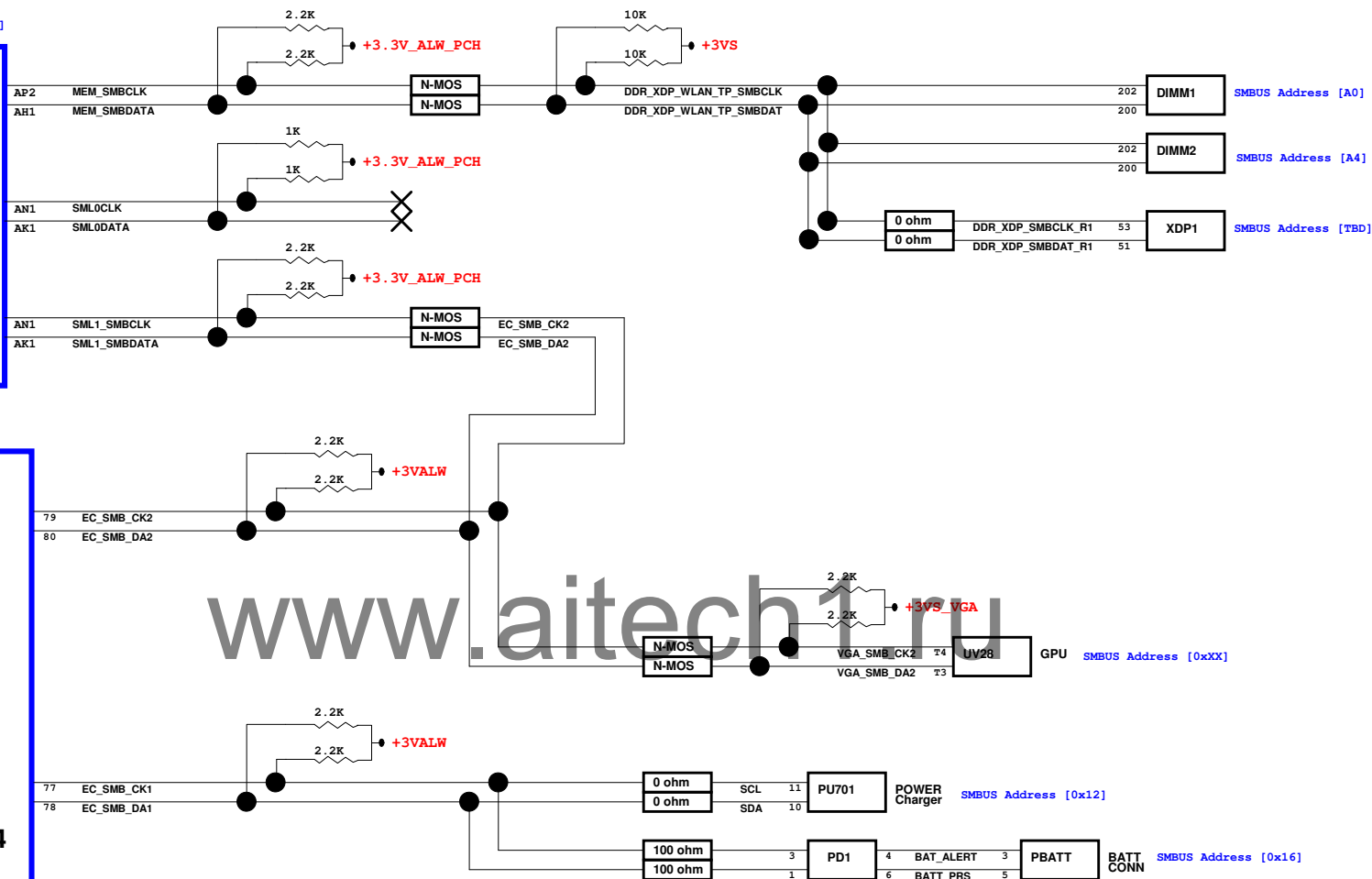
SATA

SATA0	HDD
SATA1	
SATA2	
SATA3	

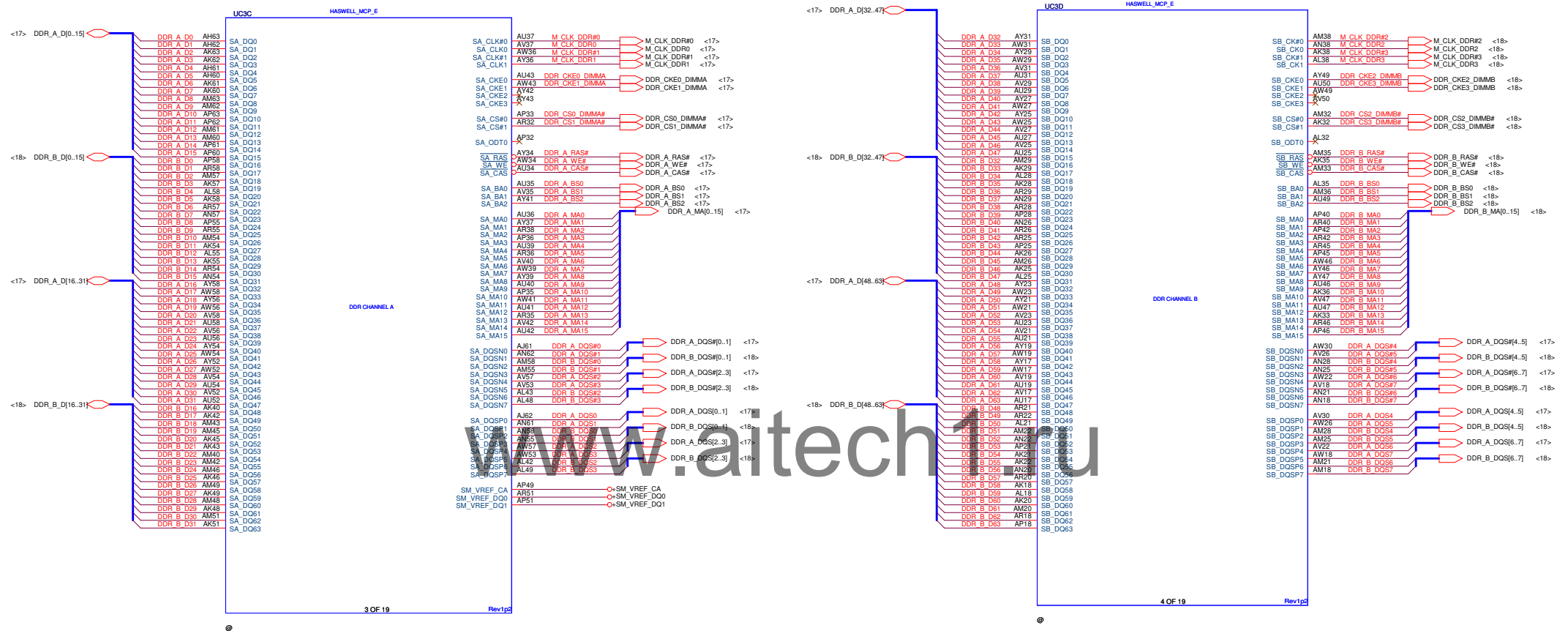
SMBUS Address [0x9a]

MCH
Shark bay

KBC
KB9012A4

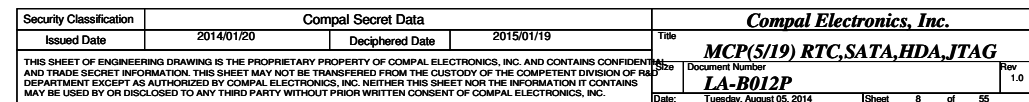


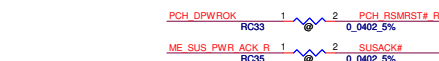
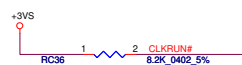
Interleaved Memory



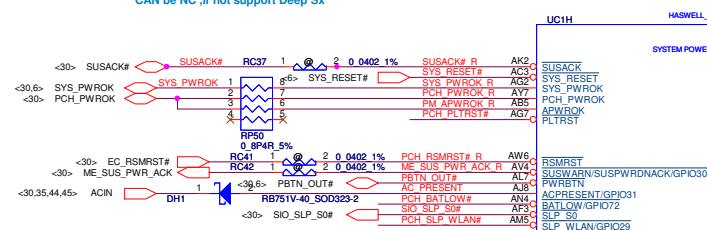
confirm by intel request PDG P141

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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	MCP(3,4/19) DDR3	
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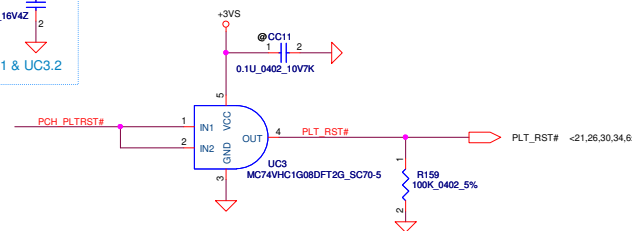
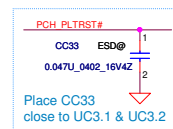




Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit
CAN be NC ,if not support Deep Sx

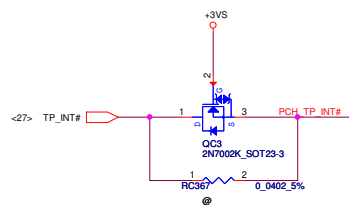
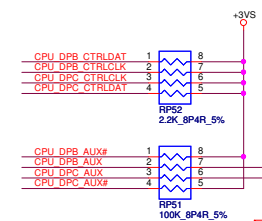
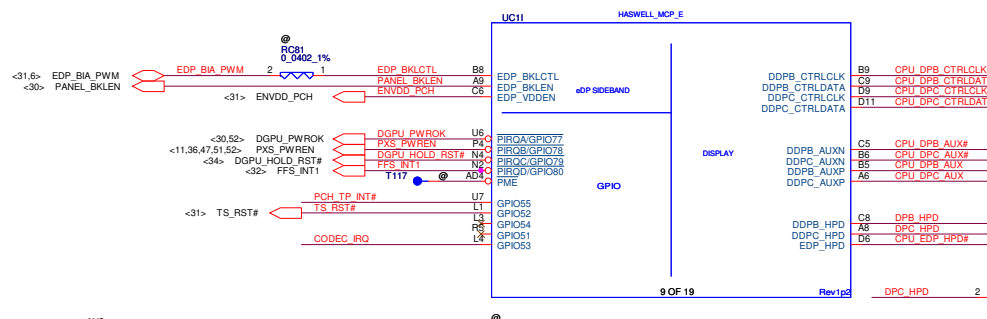
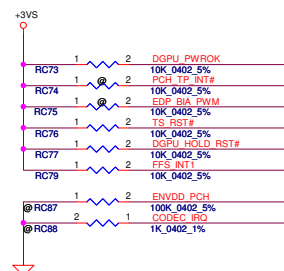
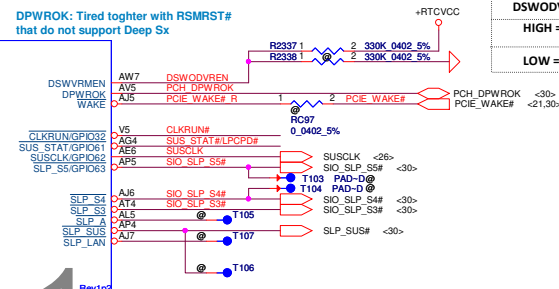


PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)

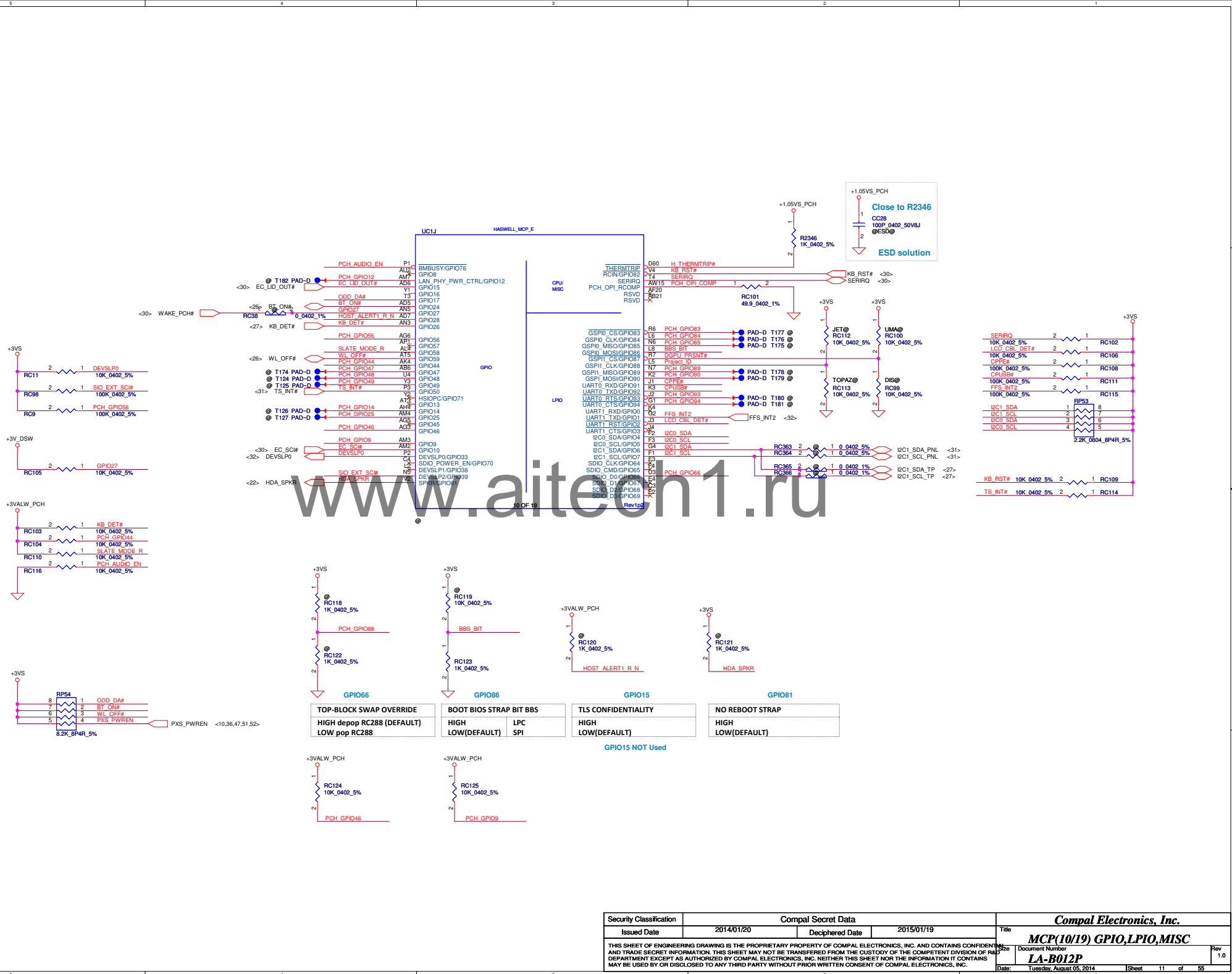


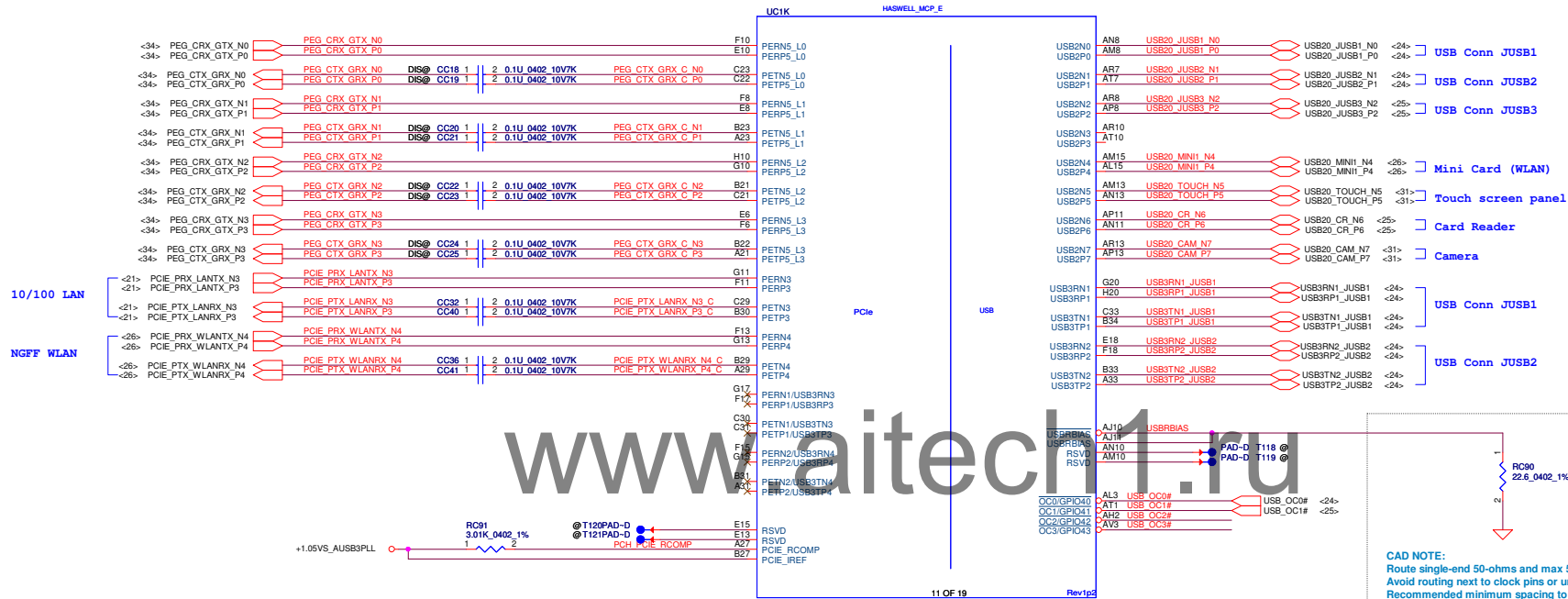
DSWODVREN - On Die DSW VR Enable
 * H : Enable(DEFAULT)
 L : Disable

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

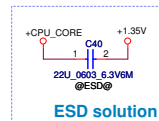
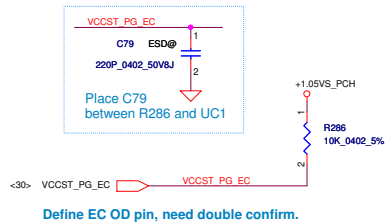


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					Document Number	
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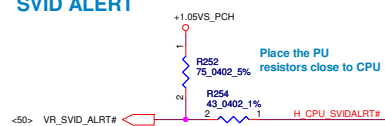




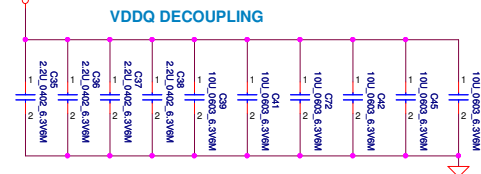
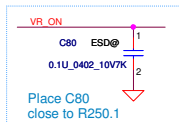
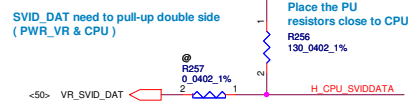
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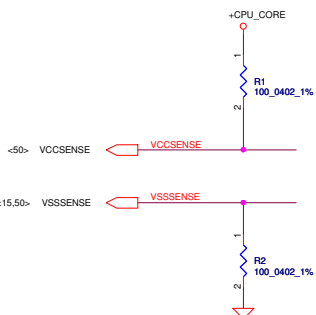
SVID ALERT



SVID DATA

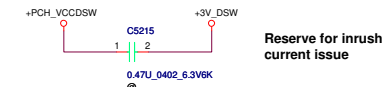
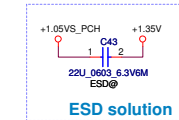
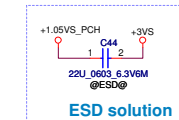
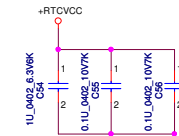
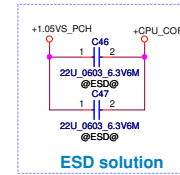
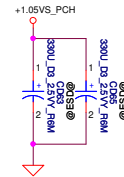
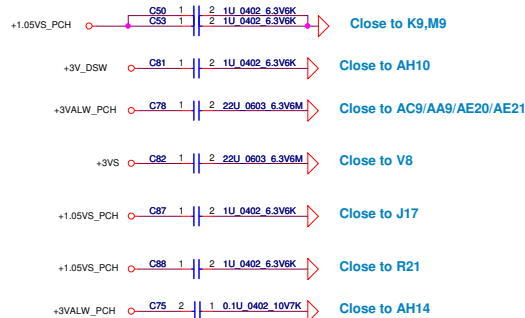
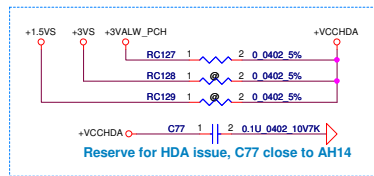
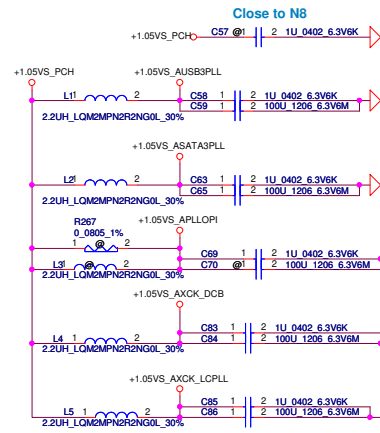


+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

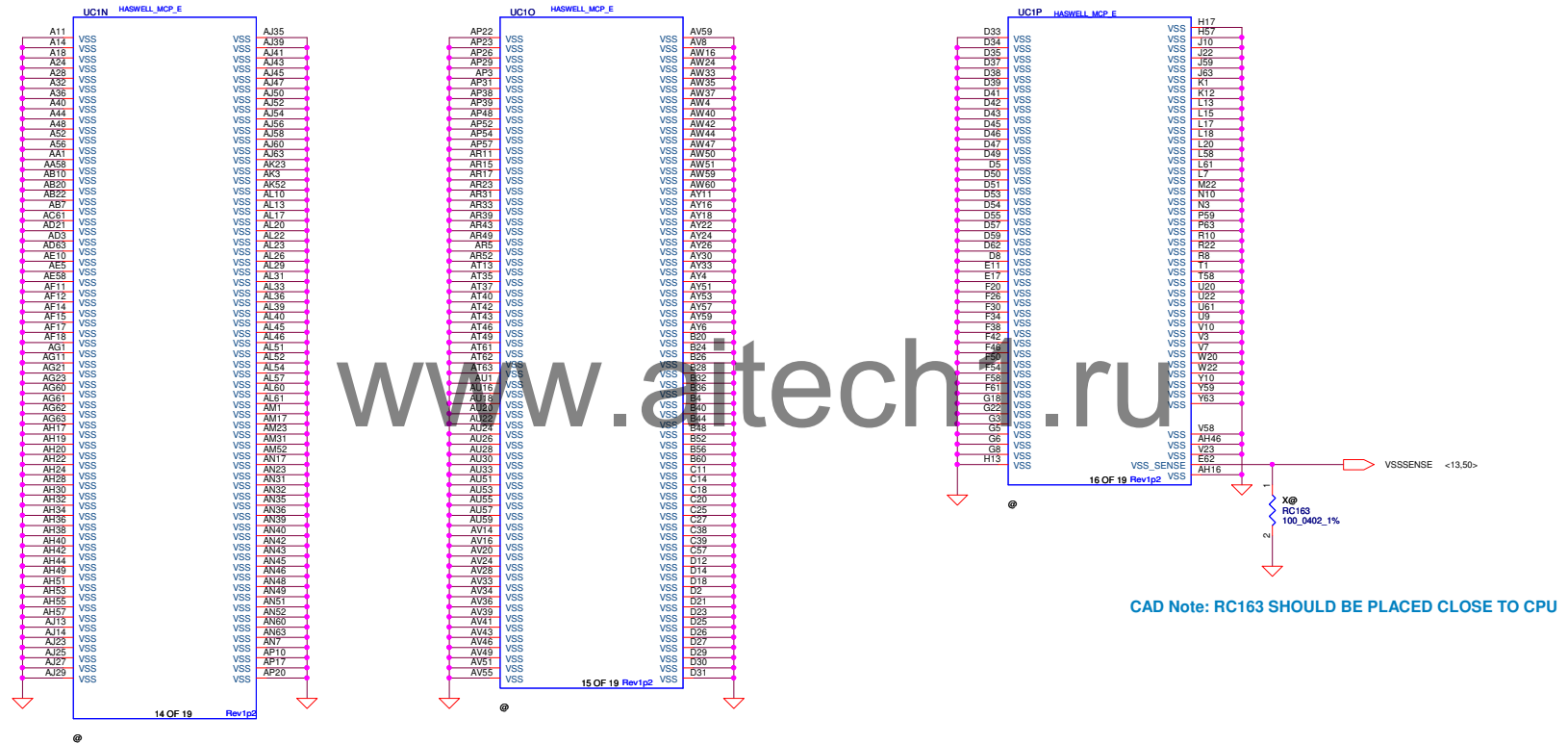


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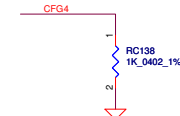
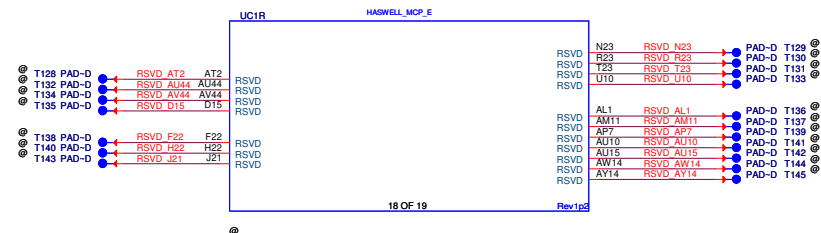
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Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

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						Document Number
LA-B012P						1.0
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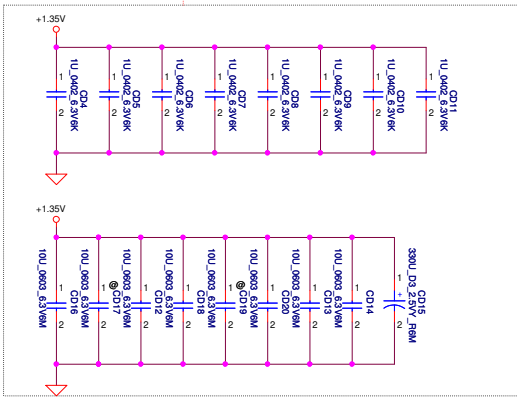
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_A_DQ# [0..7]
<7> DDR_A_DQ [0..63]
<7> DDR_A_DQS [0..7]
<7> DDR_A_MA [0..15]

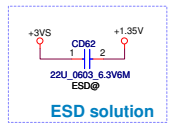
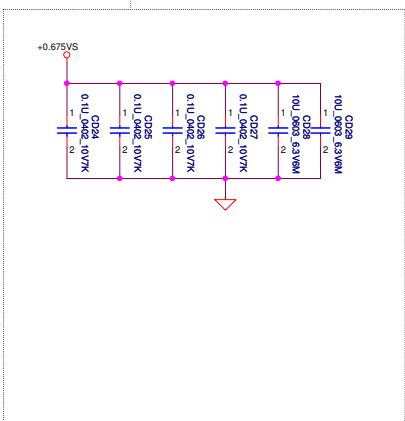
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

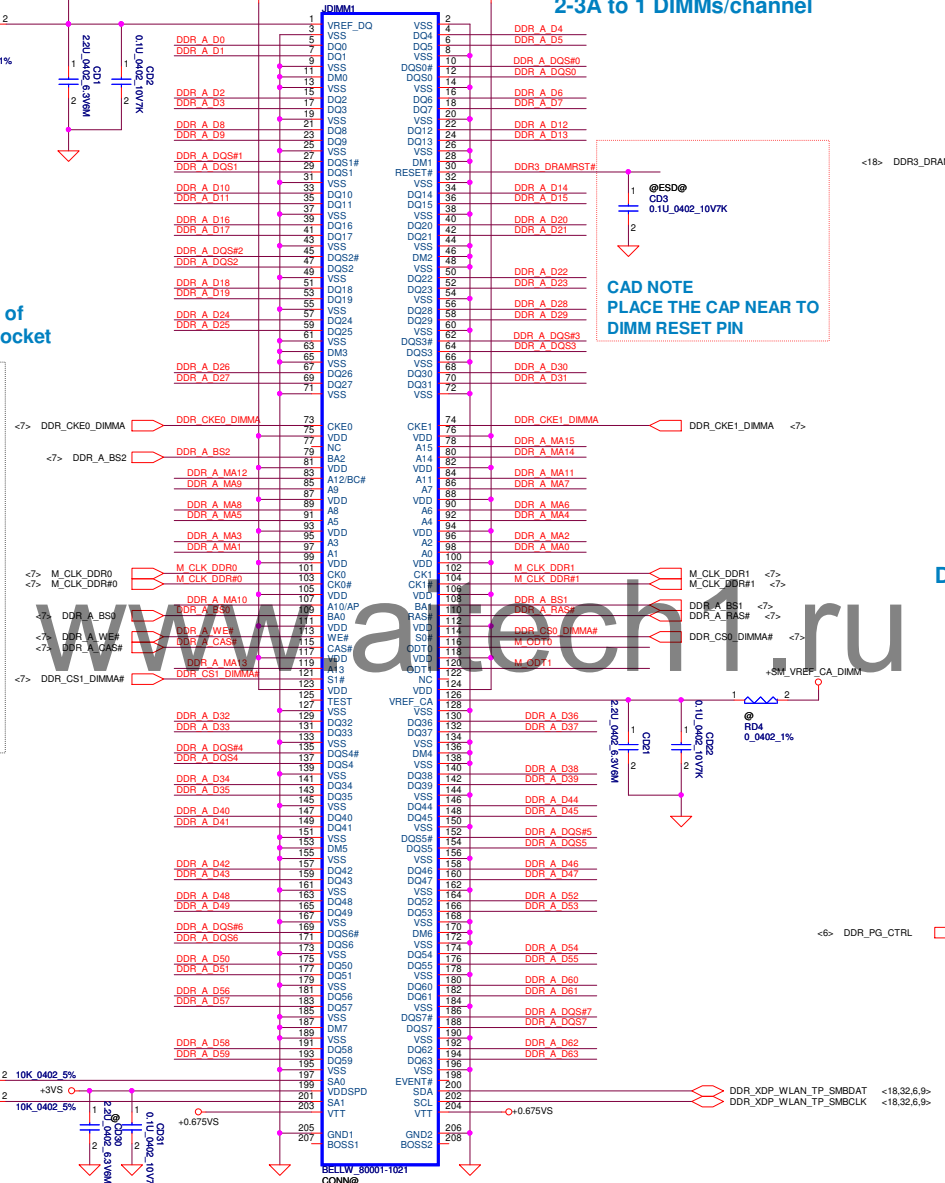


Layout Note:
Place near JDIMM1. 203, 204



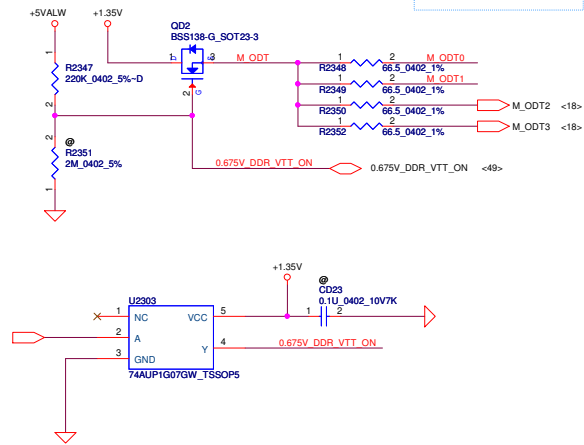
H=4mm

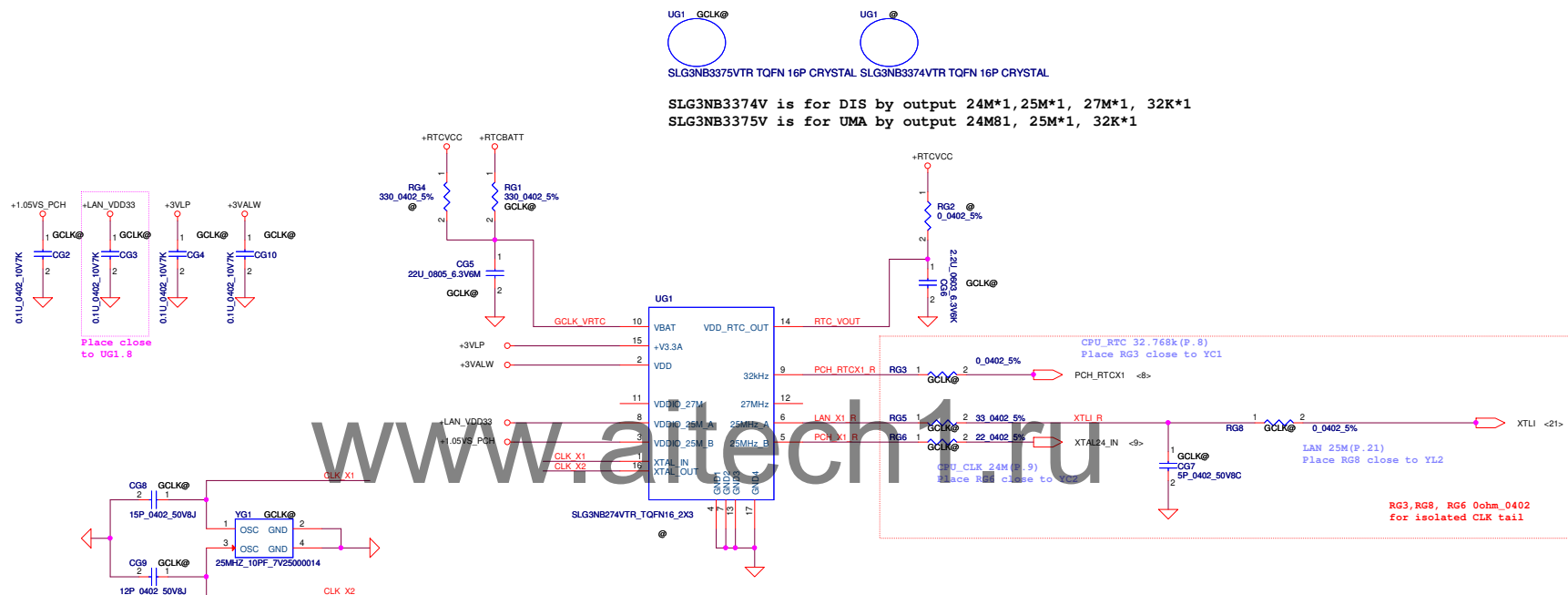
2-3A to 1 DIMMs/channel

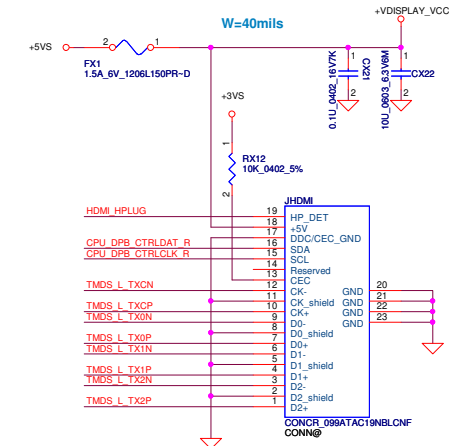
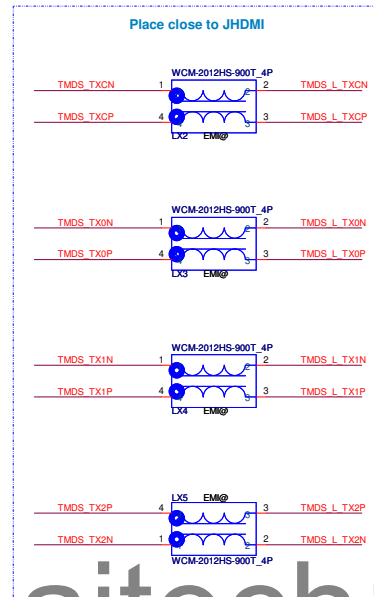
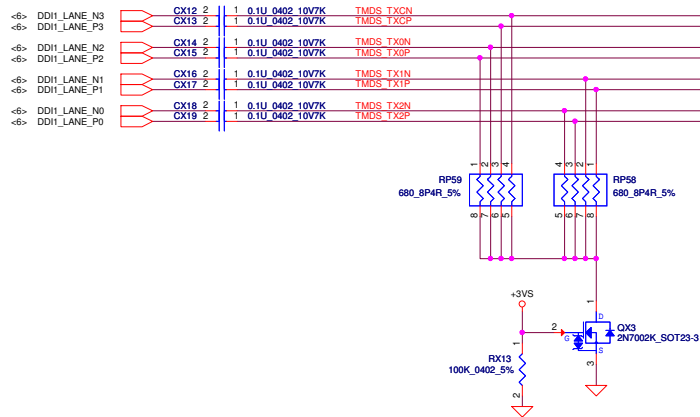


CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

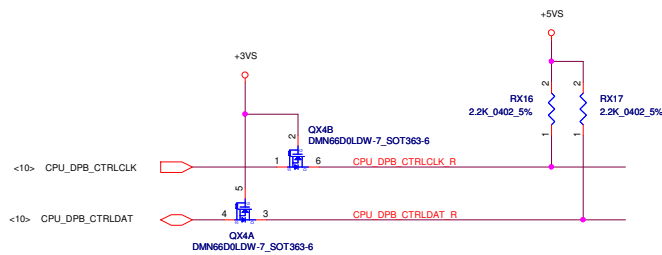
DDR3L SODIMM ODT GENERATION



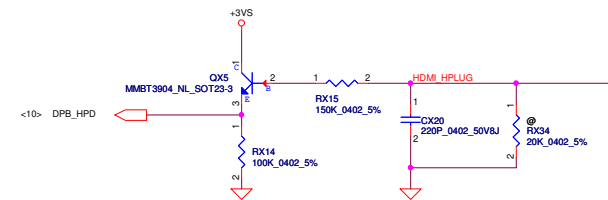




Part Number	Description
8000000002BH	ROYALTY HDMI W/LOGO
8000000002BH	HDMI W/Logo:8000000002BH



TMSD_L_TXCN	@EMI@	CX23	1	2	3.3P_0402_50V8C
TMSD_L_TXCP	@EMI@	CX24	1	2	3.3P_0402_50V8C
TMSD_L_TX0N	@EMI@	CX25	1	2	3.3P_0402_50V8C
TMSD_L_TX0P	@EMI@	CX26	1	2	3.3P_0402_50V8C
TMSD_L_TX1N	@EMI@	CX27	1	2	3.3P_0402_50V8C
TMSD_L_TX1P	@EMI@	CX28	1	2	3.3P_0402_50V8C
TMSD_L_TX2N	@EMI@	CX29	1	2	3.3P_0402_50V8C
TMSD_L_TX2P	@EMI@	CX30	1	2	3.3P_0402_50V8C



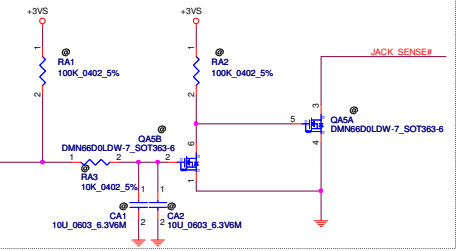
CA71, CA51 place close to Pin 26

CA3, CA5 change Value
from 10U_0603_6.3V6M to
4.7U_0603_6.3V6K

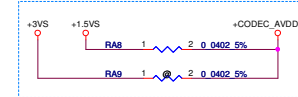
CA57, CA58 close
to UA1 pin1

CA59 CA60 close
to UA1 pin9

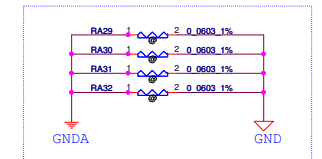
JACK_PLUG Delay circuitis



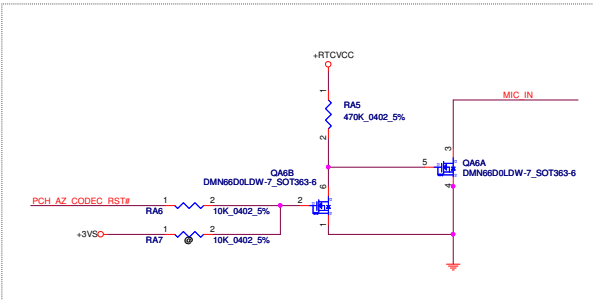
Reserve for HDA issue



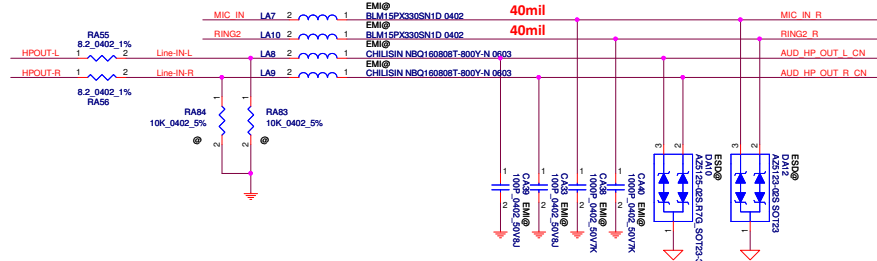
Reserve for cancel Delay circuitis



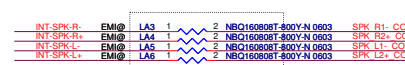
Place on the moat between GND & GNDA.



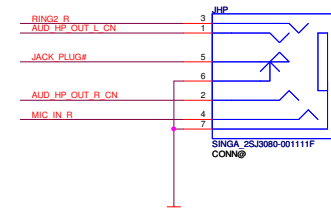
iPhone and Nokia type Combo Jack



Close to UA1
Pin11,13,14,16



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

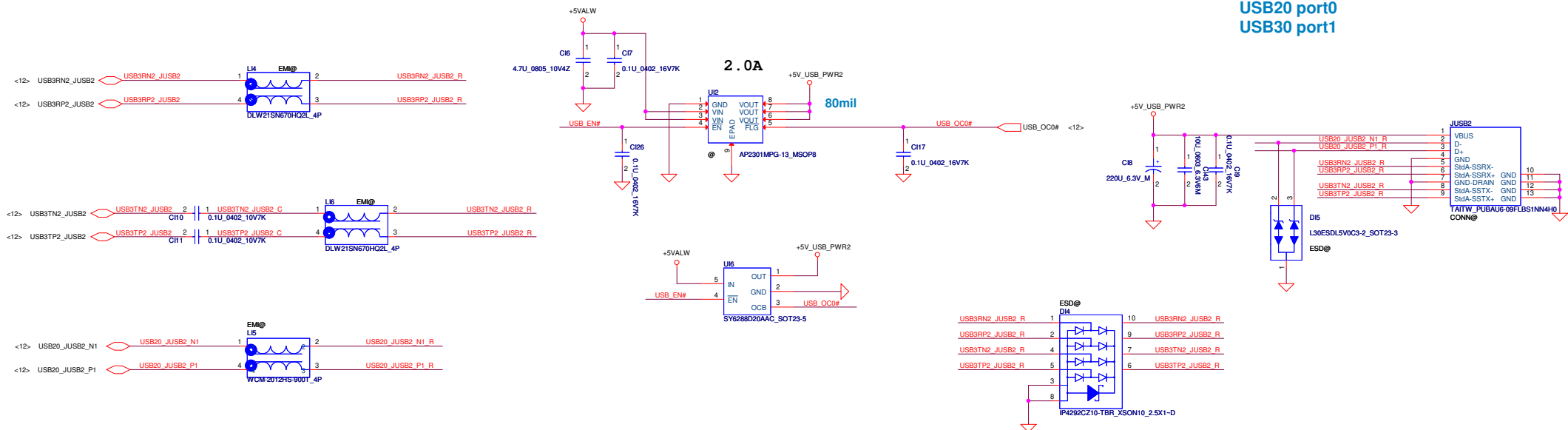
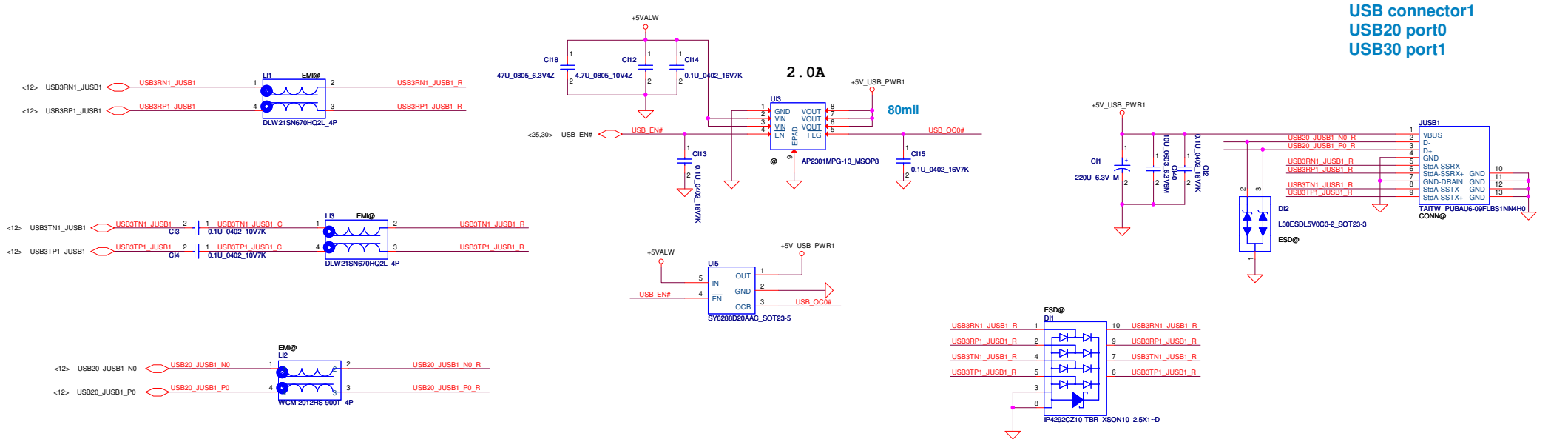


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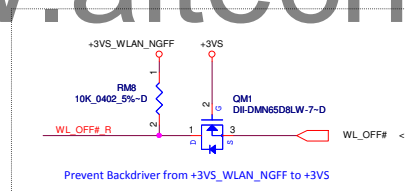
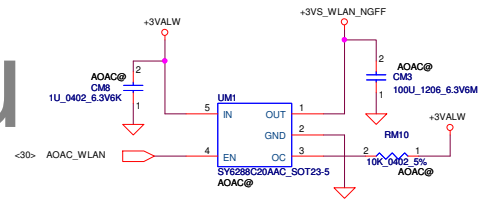
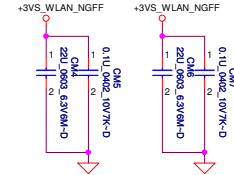
Security Classification		Compal Secret Data		Title	
Issued Date		2014/01/20	Deciphered Date	2015/01/19	
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				LA-B012P	1.0
Date: Tuesday, August 05, 2014				Sheet	23 of 55

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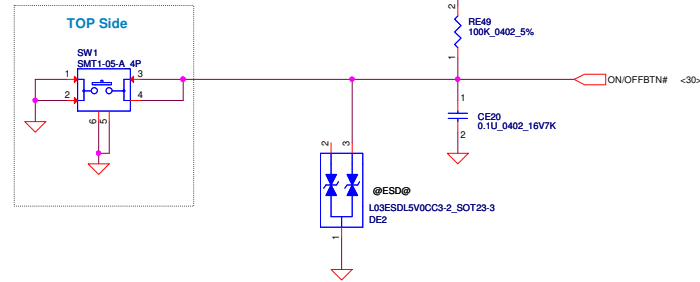
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Issued Date		2014/01/20	Deciphered Date	2015/01/19	Title	
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					Docuement Number	Rev
					LA-B012P	1.0
					Date	Tuesday, August 05, 2014

closed to pin 2, 4 closed to pin 64, 66

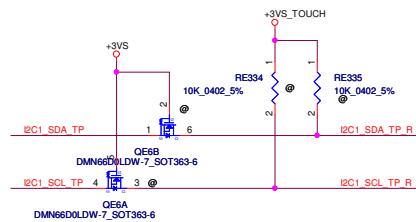
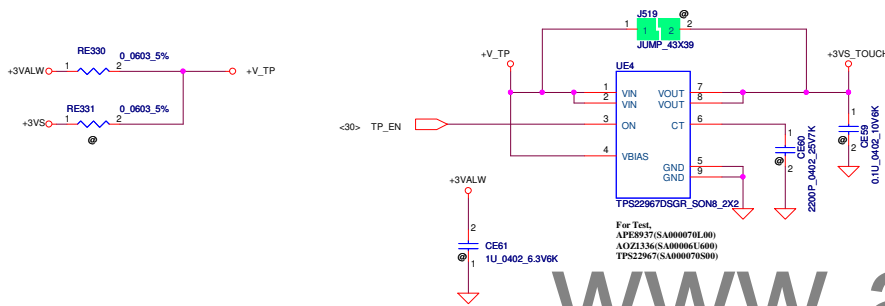


Power ON Circuit

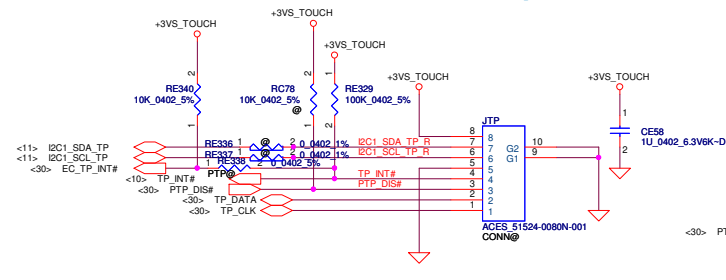
ON/OFF switch



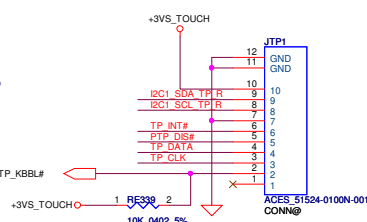
J519 short



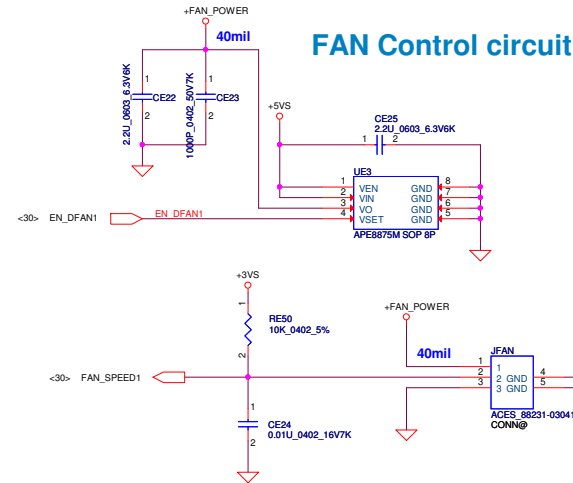
Touch pad



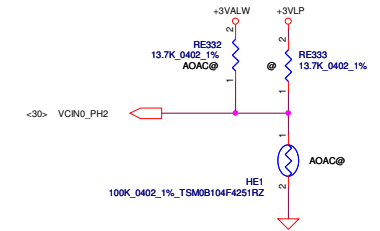
PTP



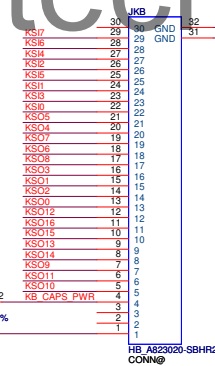
FAN Control circuit



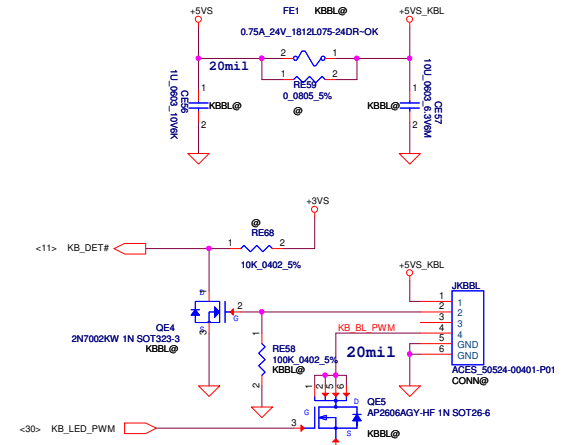
HE1 place around FAN area.



INT_KBD Connector

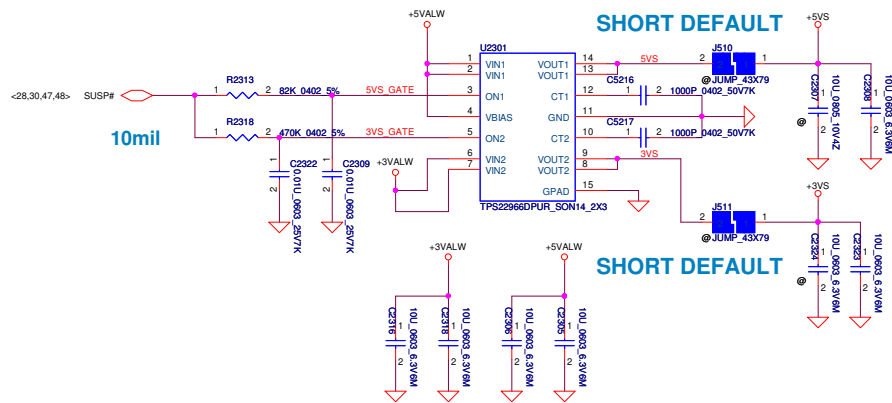


* Key Board Back Light

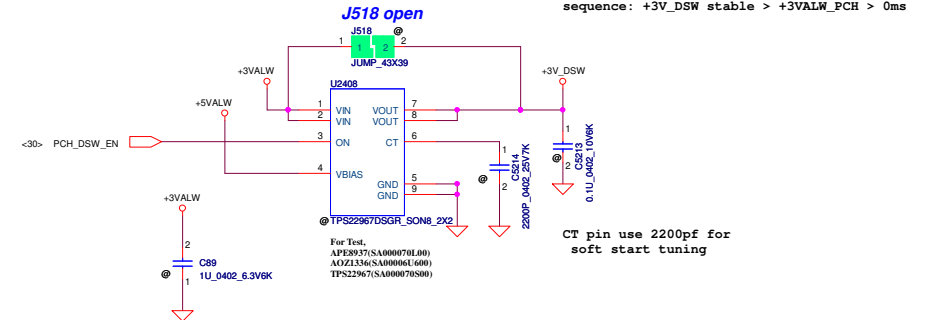


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Date		Tuesday, August 05, 2014		Sheet 27 of 55	

+5VS and +3VS switch

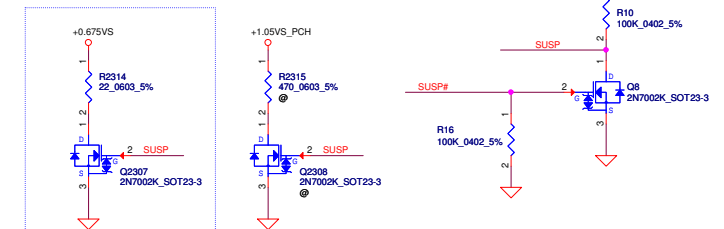
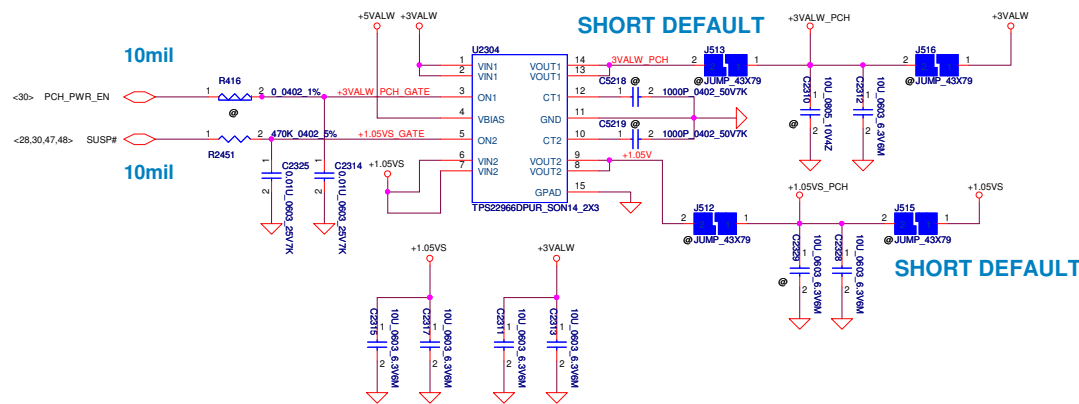


+3VALW TO +3V_DSW



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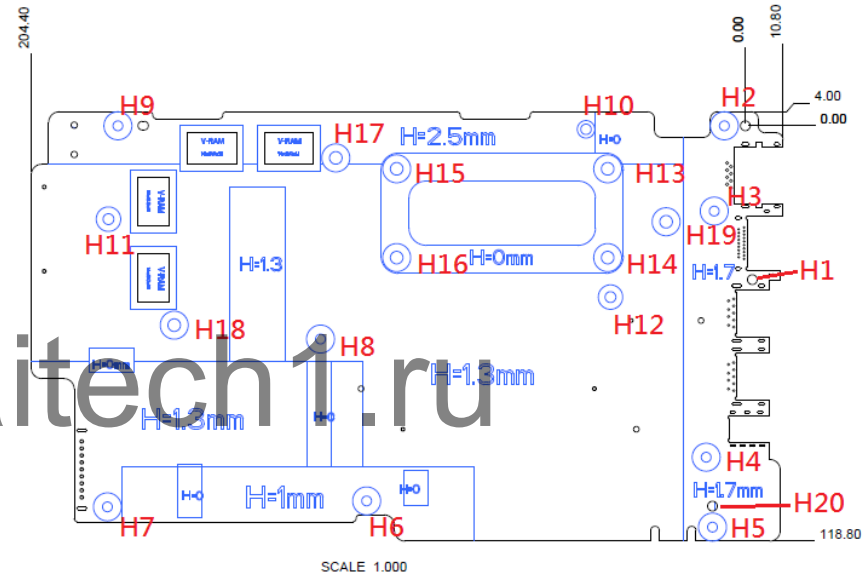
+3VALW_PCH switch



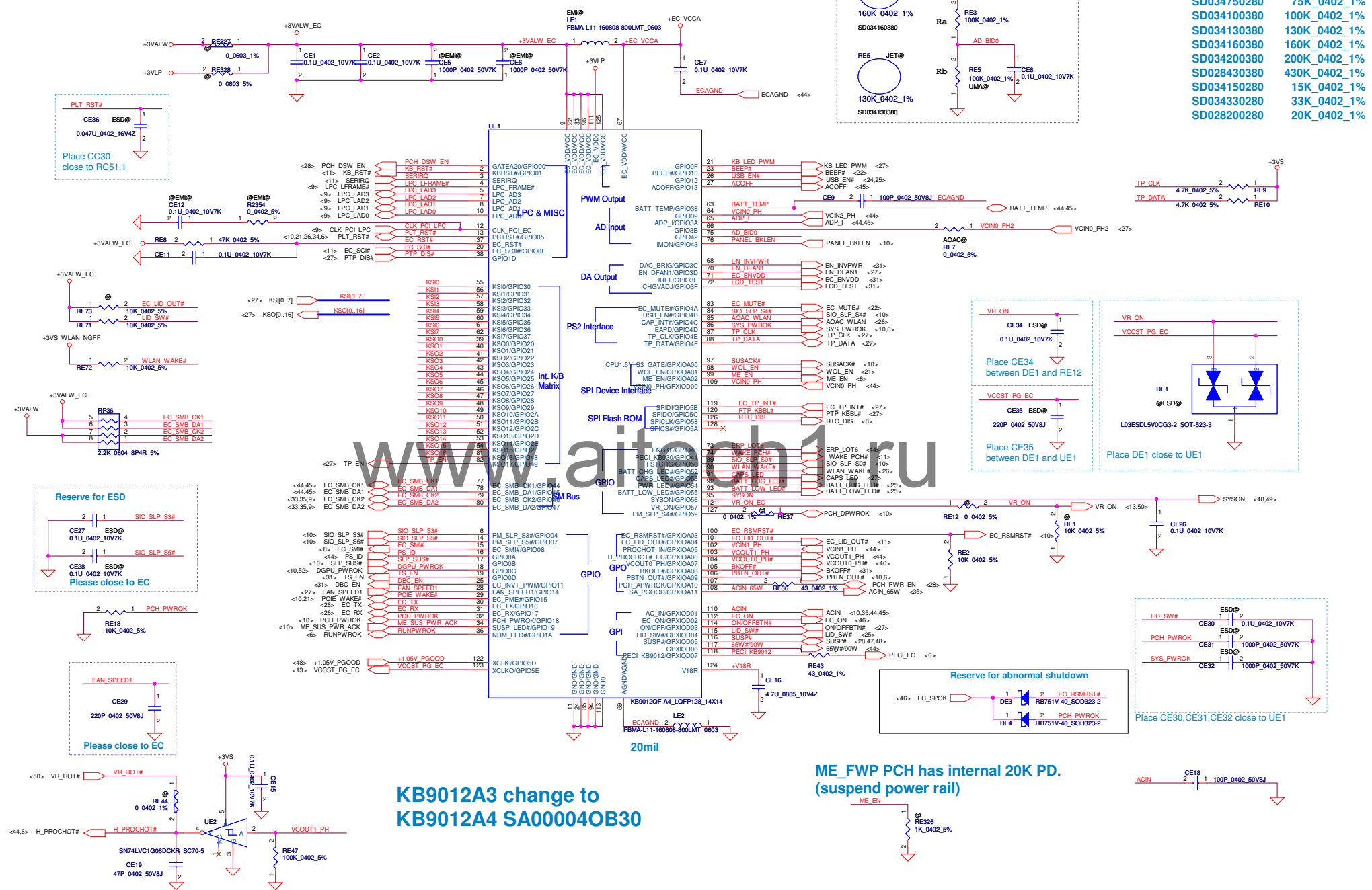
For Intel S3 Power Reduction

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				Date	Tuesday, August 05, 2014
				Sheet	28 of 55
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ZZZ
PCB 13P LA-B011P REV0 M/B
DA60013U000

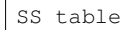


Security Classification		Compal Secret Data		Compal Electronics, Inc. Screw Hole	
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				Date: Tuesday, August 05, 2014	Sheet 29 of 55

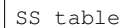


SD034120280	12K_0402_1%
SD034270280	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD028430380	430K_0402_1%
SD034150280	15K_0402_1%
SD034330280	33K_0402_1%
SD028200280	20K_0402_1%

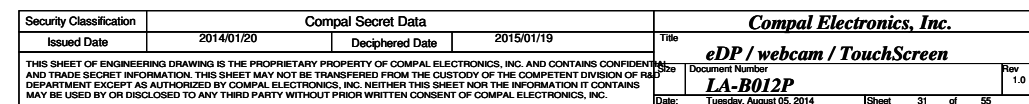
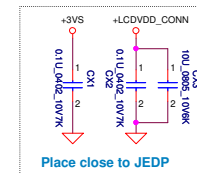
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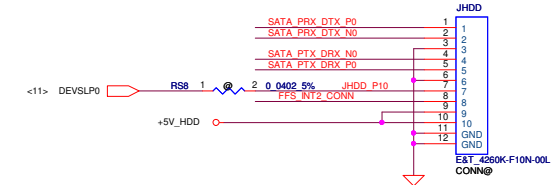
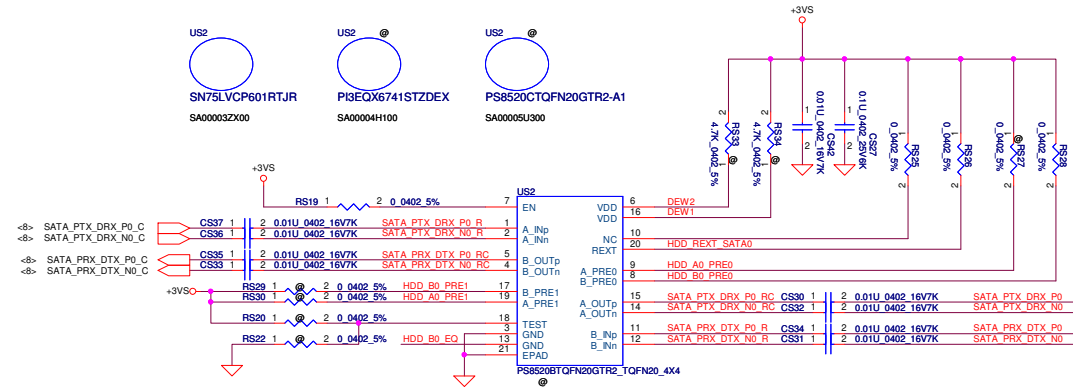
LCD backlight PWR CTRL



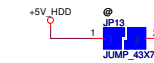
eDP Connector



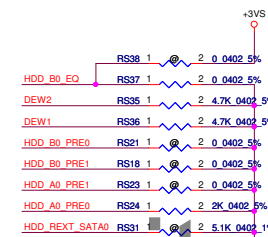
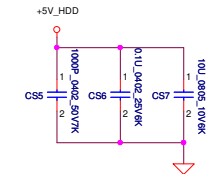
SATA HDD Connector



+5V_HDD Source



SHORT DEFAULT



Pin 20:
PARADE PS8250B:
Depop RS26

PERICOM PI3EQX6741ST:
Pop RS26

ASMEDIA ASM1466:
Pop RS26

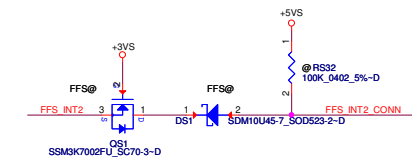
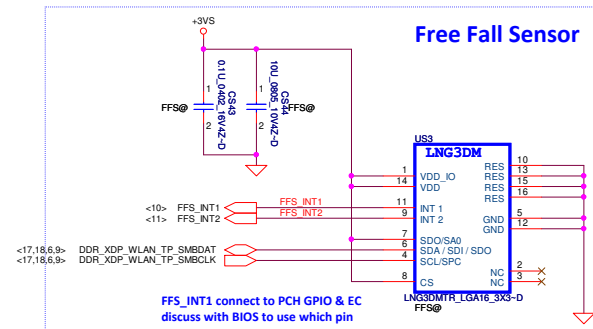
Pin 9:
PARADE PS8250B:
Depop RS24.

PERICOM PI3EQX6741ST:
Depop RS24

ASMEDIA ASM1466:
Pop RS24 to pull down

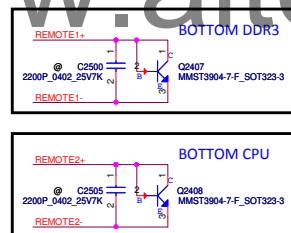
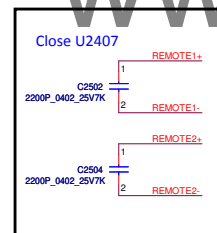
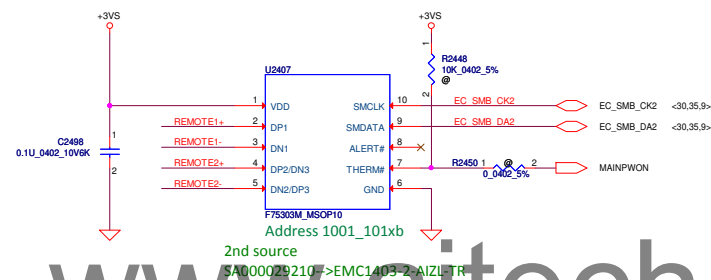
ASMEDIA ASM1466:
Pop RS24 to pull down

Free Fall Sensor



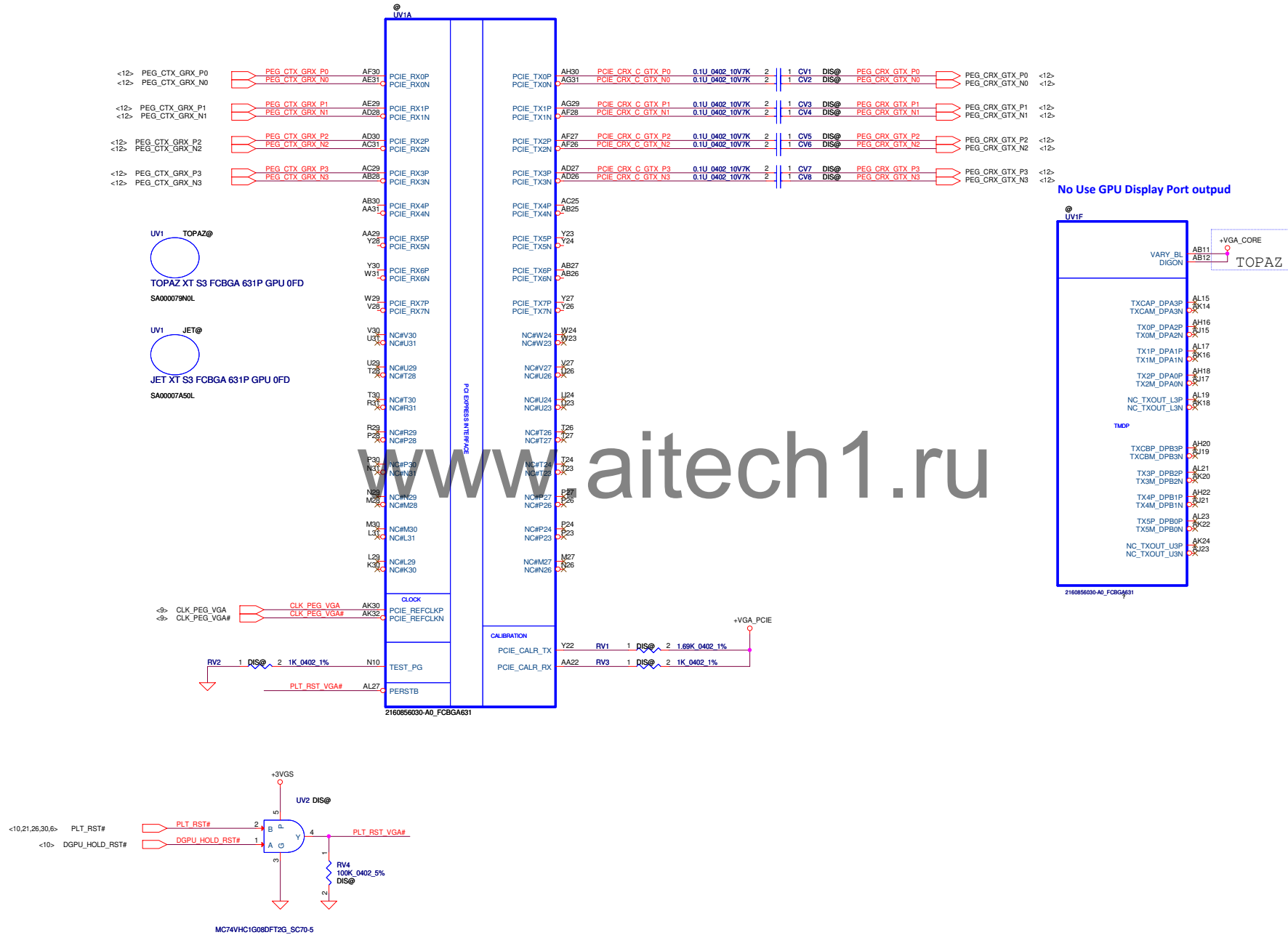
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Fintek thermal sensor
placed near by TOP DDR3



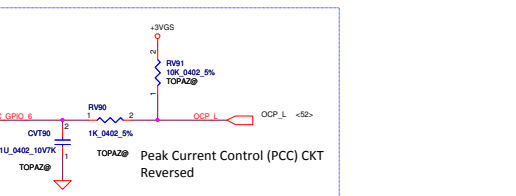
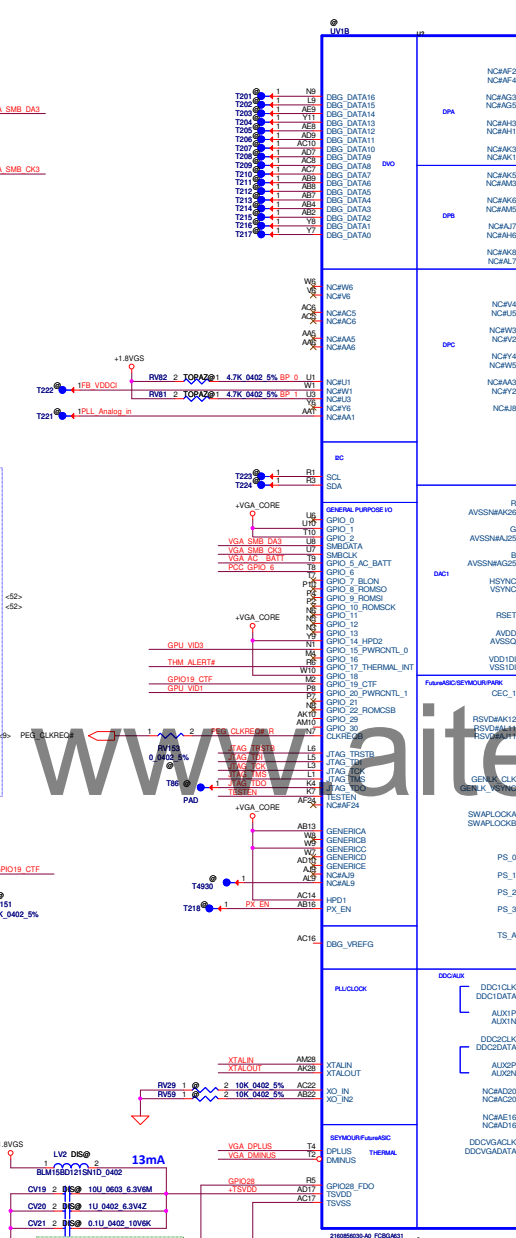
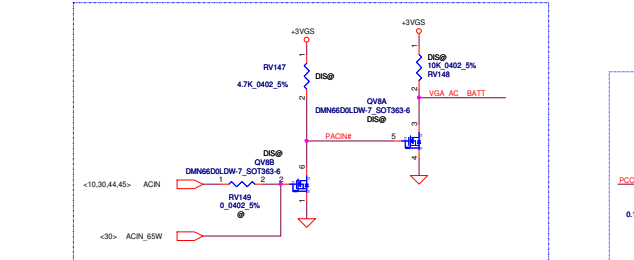
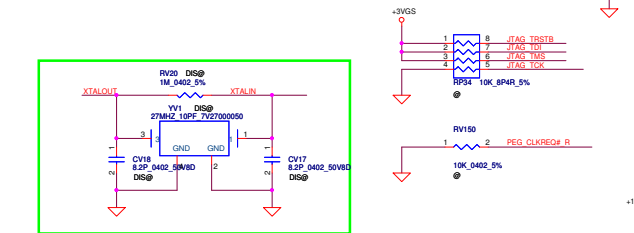
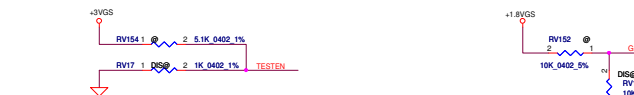
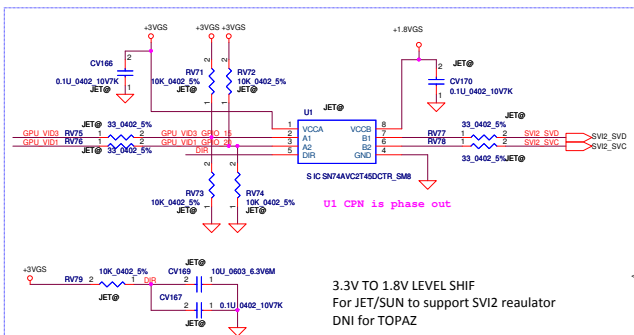
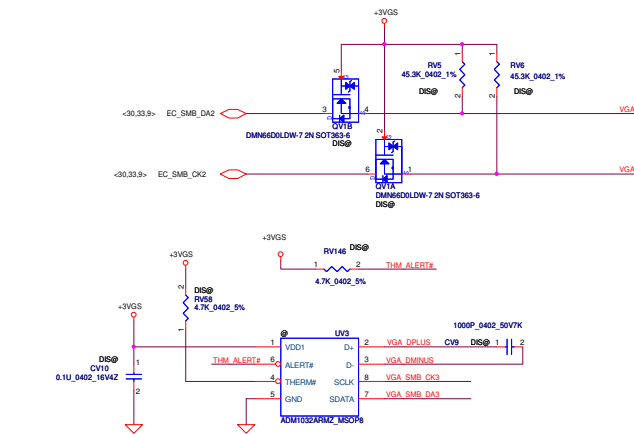
REMOTE1.2 (+/-):
Trace width/space:10/10 mil
Trace length:<8"

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No Use GPU Display Port output

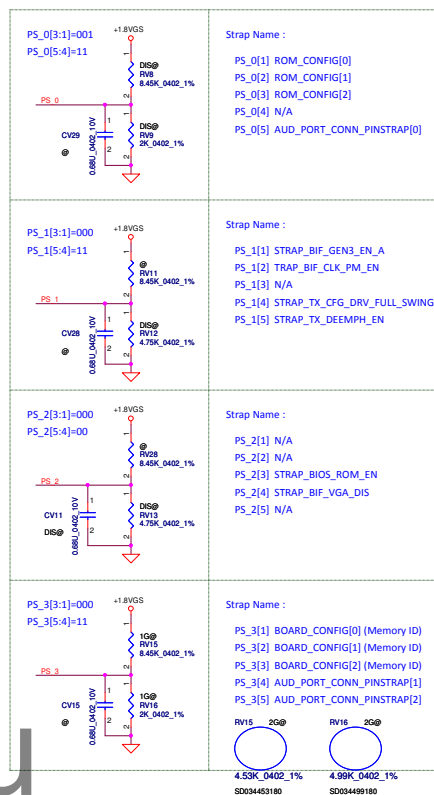
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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Size	Document Number
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Resistor Divider Lookup Table			
R_u (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

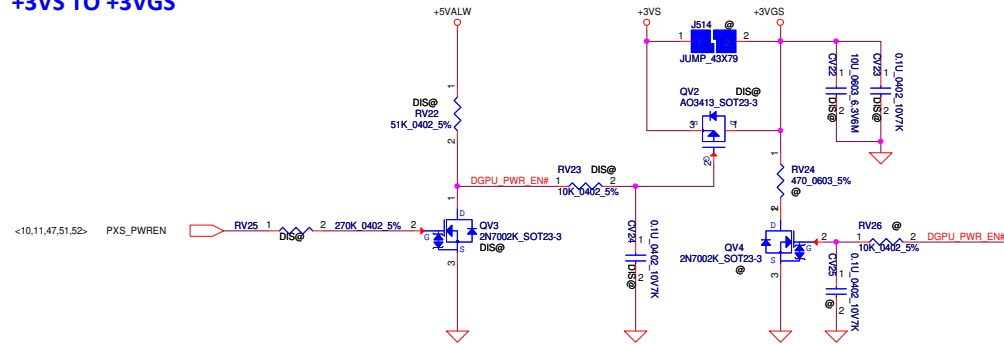
Capacitor Divider Lookup Table		
Cap (nF)	Bitd [5:4]	
680nF	00	
82nF	01	
10nF	10	
NC	11	

0402 1% resistors are required

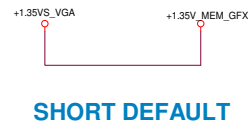


Memory ID	P/N	Vendor	Configuration	Size
(default) 000	SA000068UOL	SAMSUNG	K4W2G1646Q-BC1A	1GB
001	SA00006H4OL	HYNIX	H5TC2G63FFR-11C	1GB
010	SA0000675OL	Micron	MT41J128M16/T-093G	1GB
011	SA000076POL	SAMSUNG	K4W4G1646B-HC11	2GB
(default) 100	SA00006E8OL	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077KOL	Micron	MT41J256M16HA-093G	2GB

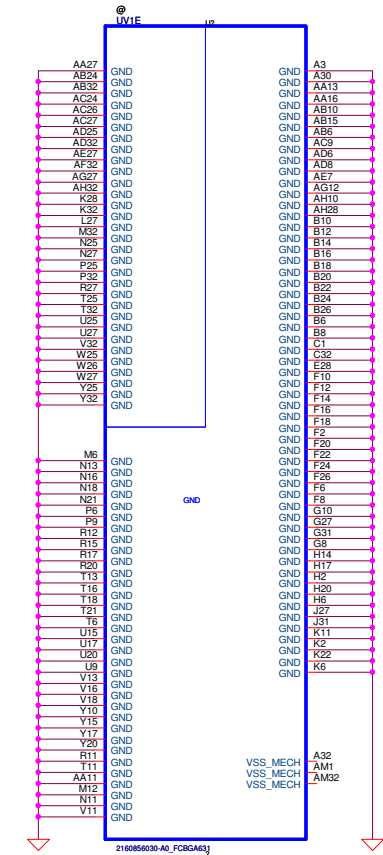
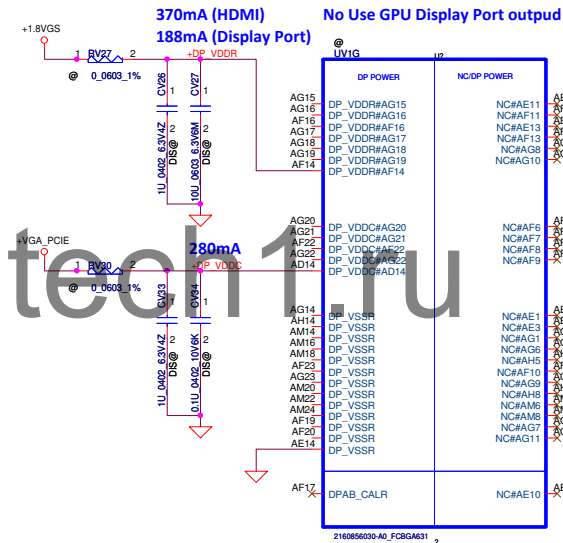
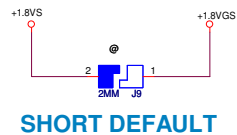
+3VS TO +3VGS



+1.35VS_VGA TO +1.35V_MEM_GFX

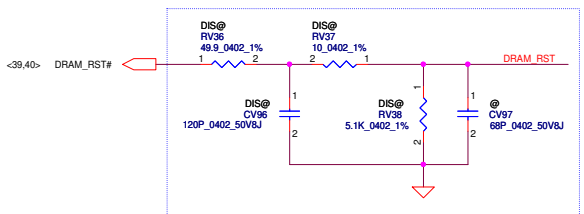
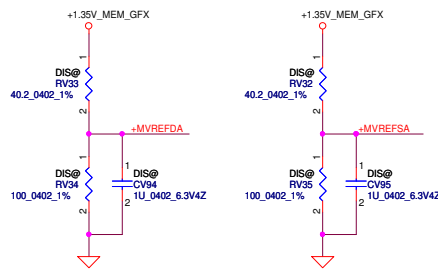


+1.8VS TO +1.8VGS

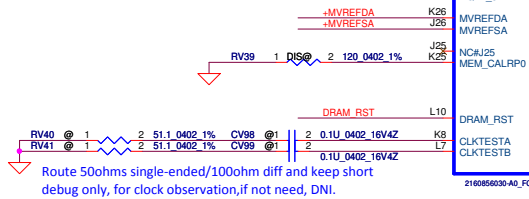


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						TOPAZ Power/GND
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						Rev 1.0
Date: Tuesday, August 05, 2014						Sheet 36 of 55

<39,40> M_DA[63..0] M_DA[63..0]
<39,40> M_MA[15..0] M_MA[15..0]
<39,40> M_DM[7..0] M_DM[7..0]
<39,40> M_DS[7..0] M_DS[7..0]
<39,40> M_DS#[7..0] M_DS#[7..0]



Place close to GPU (within 25mm)
and place component close to each other

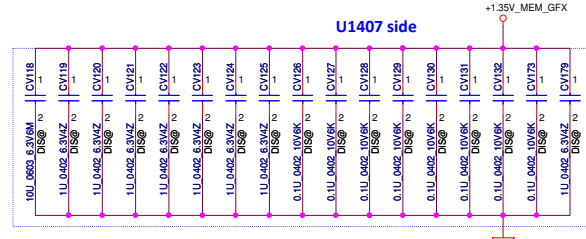
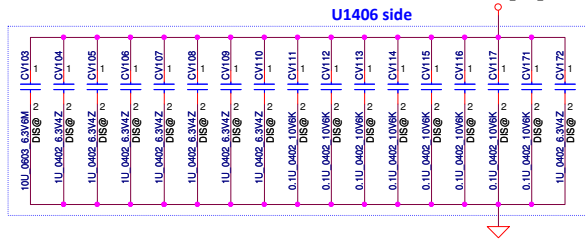
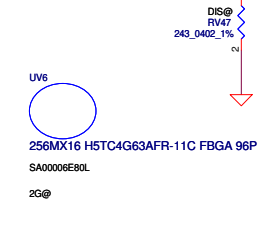
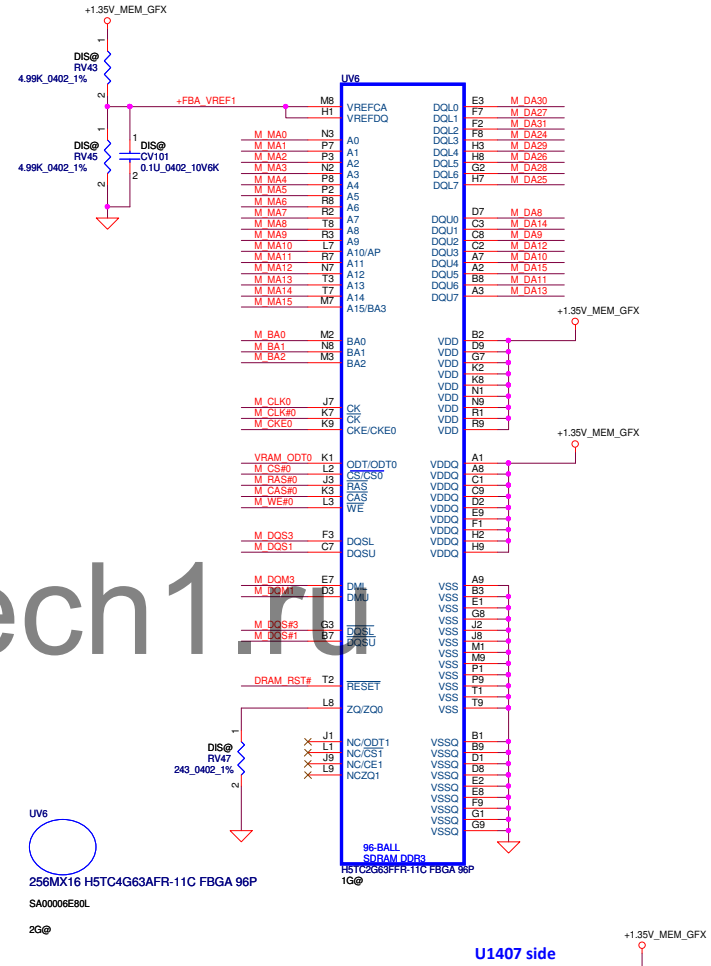
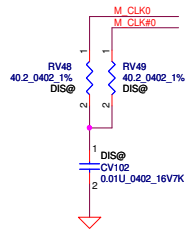
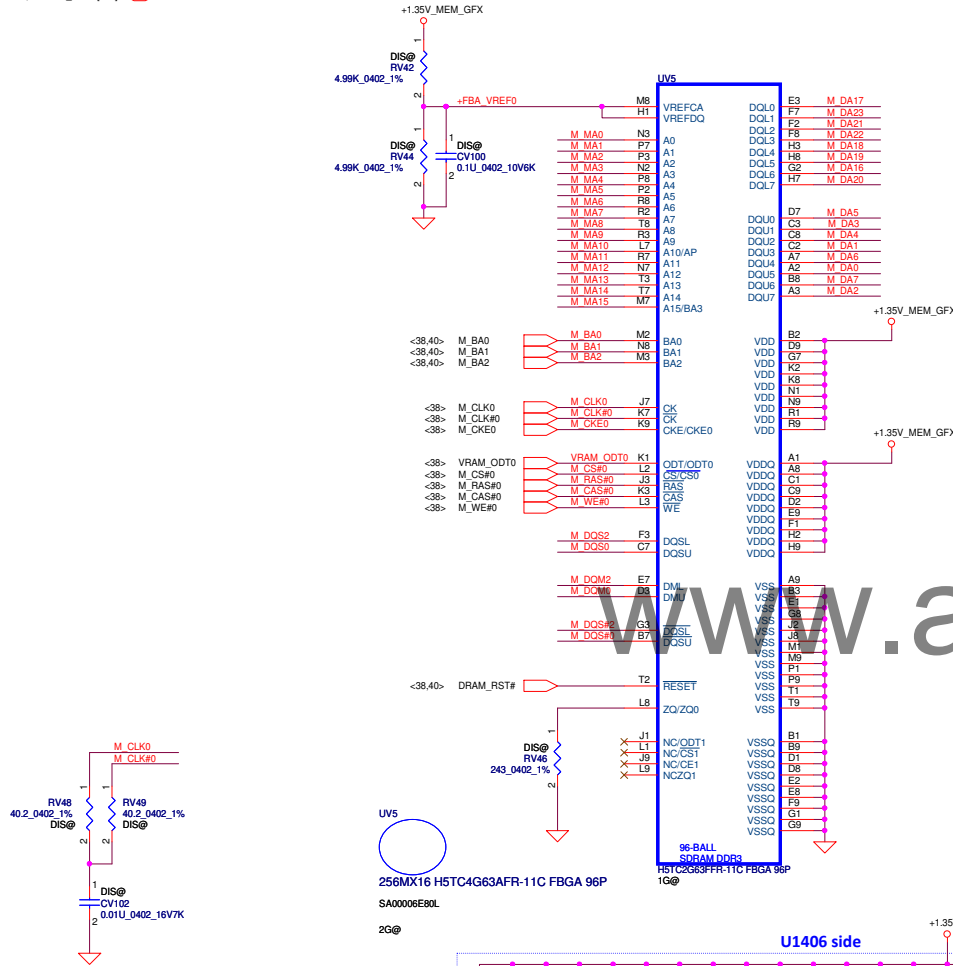


Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

GPIO		GPIO		GPIO	
M_DA0	K27	QDA0_0	MAA0_0/MAA_0	M_MA0	K17
M_DA1	J29	QDA0_1	MAA0_1/MAA_1	M_MA1	J20
M_DA2	H30	QDA0_2	MAA0_2/MAA_2	M_MA2	H29
M_DA3	H32	QDA0_3	MAA0_3/MAA_3	M_MA3	G23
M_DA4	G29	QDA0_4	MAA0_4/MAA_4	M_MA4	G24
M_DA5	F32	QDA0_5	MAA0_5/MAA_5	M_MA5	H24
M_DA6	F30	QDA0_6	MAA0_6/MAA_6	M_MA6	J19
M_DA7	C30	QDA0_7	MAA0_7/MAA_7	M_MA7	K19
M_DA8	F27	QDA0_8	MAA0_8/MAA_8	M_MA8	G20
M_DA9	A28	QDA0_9	MAA0_9/MAA_9	M_MA9	L17
M_DA10	C28	QDA0_10	MAA1_0/MAA_8	M_MA10	J14
M_DA11	G26	QDA0_11	MAA1_1/MAA_9	M_MA11	K14
M_DA12	D26	QDA0_12	MAA1_2/MAA_10	M_MA12	J11
M_DA13	F25	QDA0_13	MAA1_3/MAA_11	M_MA13	J13
M_DA14	C25	QDA0_14	MAA1_4/MAA_12	M_MA14	H11
M_DA15	E25	QDA0_15	MAA1_5/MAA_BA2	M_MA15	G11
M_DA16	E25	QDA0_16	MAA1_6/MAA_BA0	M_MA16	J18
M_DA17	D23	QDA0_17	MAA1_7/MAA_BA1	M_MA17	L15
M_DA18	E23	QDA0_18	MAA1_8/MAA_14	M_MA18	G14
M_DA19	F23	QDA0_19	MAA1_9/RSVD	M_MA19	L16
M_DA20	D22	QDA0_20	WCKA0_0/QDMA0_0	M_DM0	E32
M_DA21	F21	QDA0_21	WCKA0B_0/QDMA0_1	M_DM1	E30
M_DA22	E21	QDA0_22	WCKA0_1/QDMA0_2	M_DM2	A21
M_DA23	D21	QDA0_23	WCKA0B_1/QDMA0_3	M_DM3	C21
M_DA24	A19	QDA0_24	WCKA1_0/QDMA1_0	M_DM4	E13
M_DA25	D18	QDA0_25	WCKA1B_0/QDMA1_1	M_DM5	D12
M_DA26	F17	QDA0_26	WCKA1_1/QDMA1_2	M_DM6	E3
M_DA27	E17	QDA0_27	WCKA1B_1/QDMA1_3	M_DM7	F4
M_DA28	C17	QDA0_28	EDCA0_0/QSA0_0	M_DS0	H28
M_DA29	D16	QDA0_29	EDCA0_1/QSA0_1	M_DS1	C27
M_DA30	F15	QDA0_30	EDCA0_2/QSA0_2	M_DS2	A25
M_DA31	A15	QDA0_31	EDCA0_3/QSA0_3	M_DS3	E19
M_DA32	D14	QDA0_32	EDCA1_0/QSA1_0	M_DS4	E15
M_DA33	F13	QDA0_33	EDCA1_1/QSA1_1	M_DS5	D10
M_DA34	A13	QDA0_34	EDCA1_2/QSA1_2	M_DS6	D6
M_DA35	E13	QDA0_35	EDCA1_3/QSA1_3	M_DS7	G5
M_DA36	C13	QDA0_36	EDCA1_4/QSA1_4	M_DS8	H27
M_DA37	D12	QDA0_37	EDCA1_5/QSA1_5	M_DS9	A27
M_DA38	F11	QDA0_38	EDCA1_6/QSA1_6	M_DS10	C23
M_DA39	E11	QDA0_39	EDCA1_7/QSA1_7	M_DS11	G19
M_DA40	A11	QDA0_40	EDCA1_8/QSA1_8	M_DS12	C15
M_DA41	C11	QDA0_41	EDCA1_9/QSA1_9	M_DS13	E9
M_DA42	D10	QDA0_42	EDCA1_10/QSA1_10	M_DS14	D5
M_DA43	F10	QDA0_43	EDCA1_11/QSA1_11	M_DS15	H4
M_DA44	A10	QDA0_44	EDCA1_12/QSA1_12	M_DS16	L13
M_DA45	C10	QDA0_45	EDCA1_13/QSA1_13	M_DS17	K16
M_DA46	D10	QDA0_46	EDCA1_14/QSA1_14	M_DS18	H26
M_DA47	F10	QDA0_47	EDCA1_15/QSA1_15	M_DS19	H25
M_DA48	E10	QDA0_48	EDCA1_16/QSA1_16	M_DS20	G9
M_DA49	A10	QDA0_49	EDCA1_17/QSA1_17	M_DS21	G8
M_DA50	C10	QDA0_50	EDCA1_18/QSA1_18	M_DS22	G22
M_DA51	D10	QDA0_51	EDCA1_19/QSA1_19	M_DS23	G17
M_DA52	F10	QDA0_52	EDCA1_20/QSA1_20	M_DS24	G19
M_DA53	E10	QDA0_53	EDCA1_21/QSA1_21	M_DS25	G16
M_DA54	A10	QDA0_54	EDCA1_22/QSA1_22	M_DS26	H22
M_DA55	C10	QDA0_55	EDCA1_23/QSA1_23	M_DS27	G13
M_DA56	D10	QDA0_56	EDCA1_24/QSA1_24	M_DS28	G13
M_DA57	F10	QDA0_57	EDCA1_25/QSA1_25	M_DS29	K20
M_DA58	E10	QDA0_58	EDCA1_26/QSA1_26	M_DS30	J17
M_DA59	A10	QDA0_59	EDCA1_27/QSA1_27	M_DS31	G25
M_DA60	C10	QDA0_60	EDCA1_28/QSA1_28	M_DS32	H10
M_DA61	D10	QDA0_61	EDCA1_29/QSA1_29	M_DS33	H10
M_DA62	F10	QDA0_62	EDCA1_30/QSA1_30	M_DS34	H10
M_DA63	E10	QDA0_63	EDCA1_31/QSA1_31	M_DS35	H10

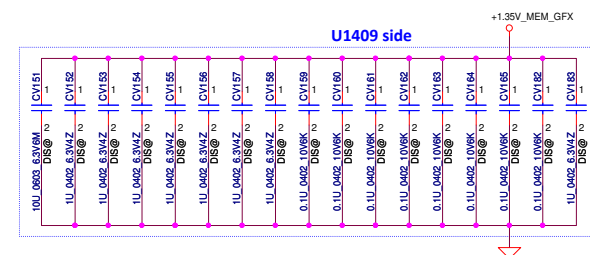
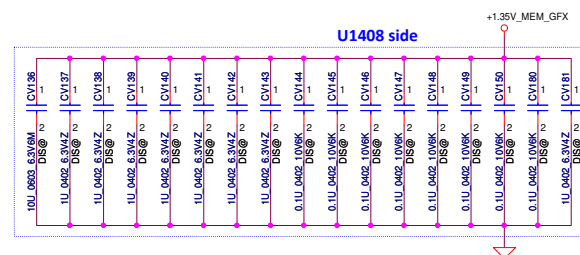
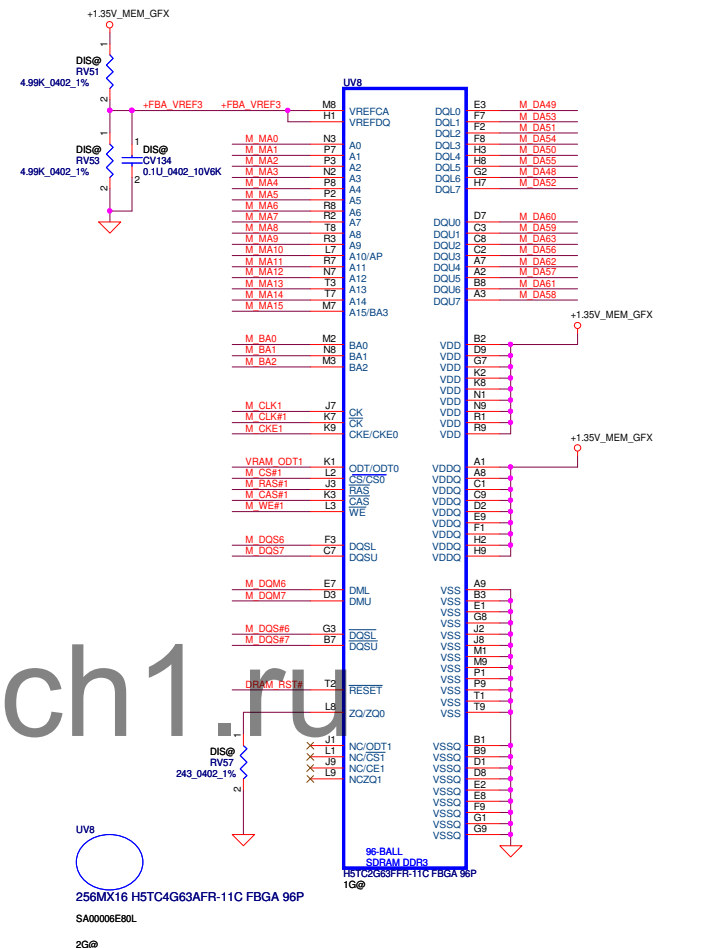
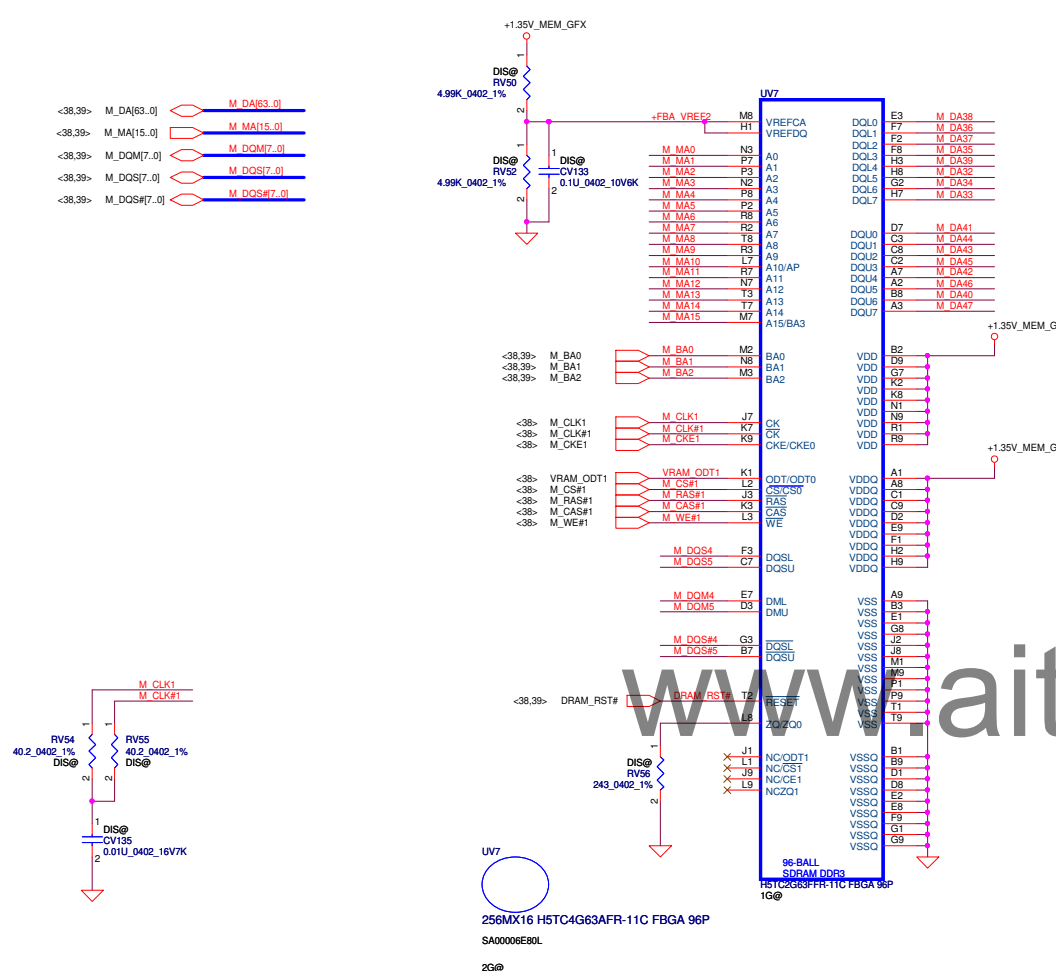
Memory Partition A - Lower 32 bits

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 <38,40> M_MA[15..0] M_MA[15..0]
 <38,40> M_DQM[7..0] M_DQM[7..0]
 <38,40> M_DQS[7..0] M_DQS[7..0]
 <38,40> M_DQS#[7..0] M_DQS#[7..0]



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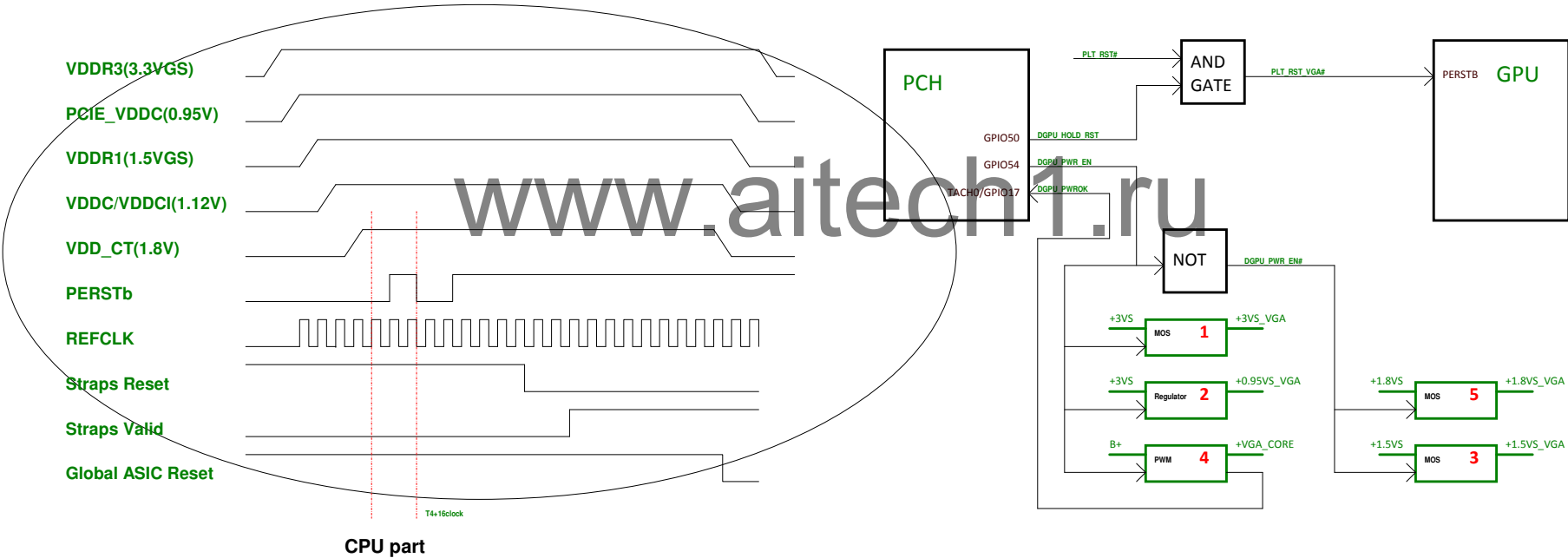
1	2
Memory Partition A - Upper 32 bits	



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						TOPAZ VRAM A Upper
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Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.

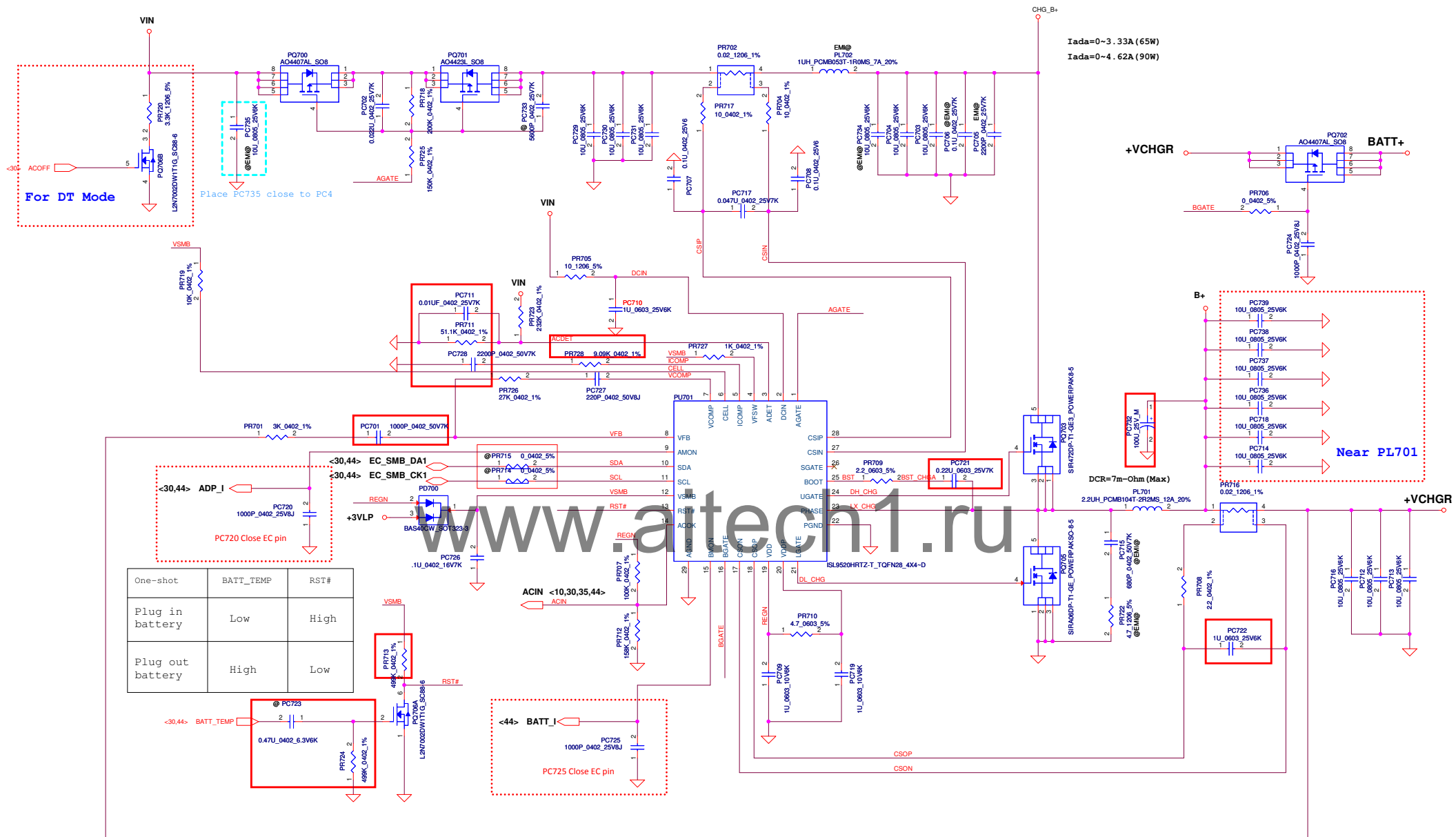


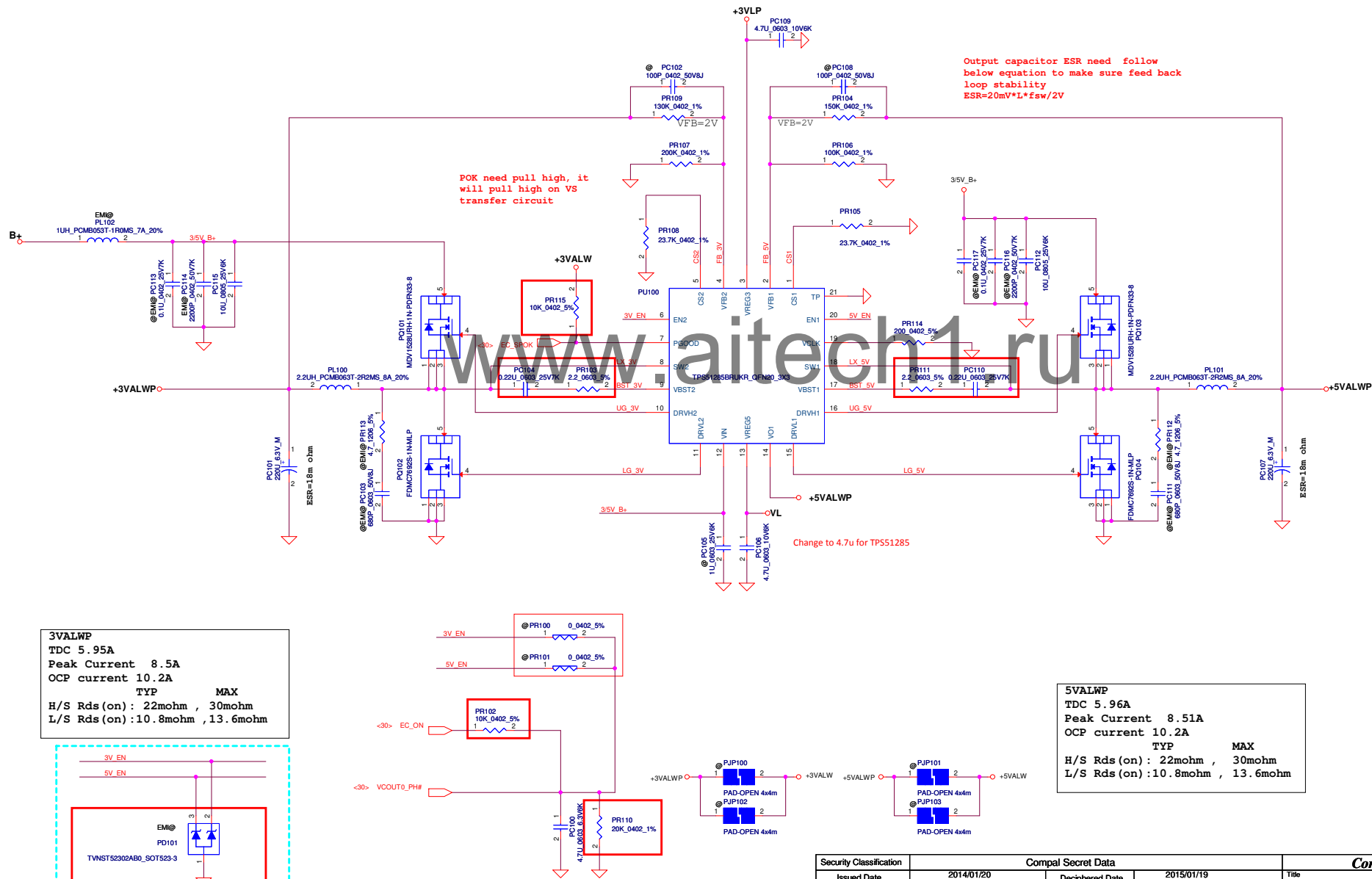
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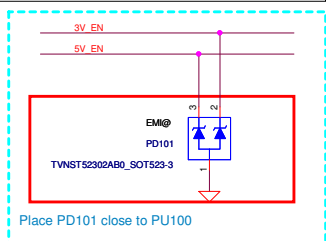
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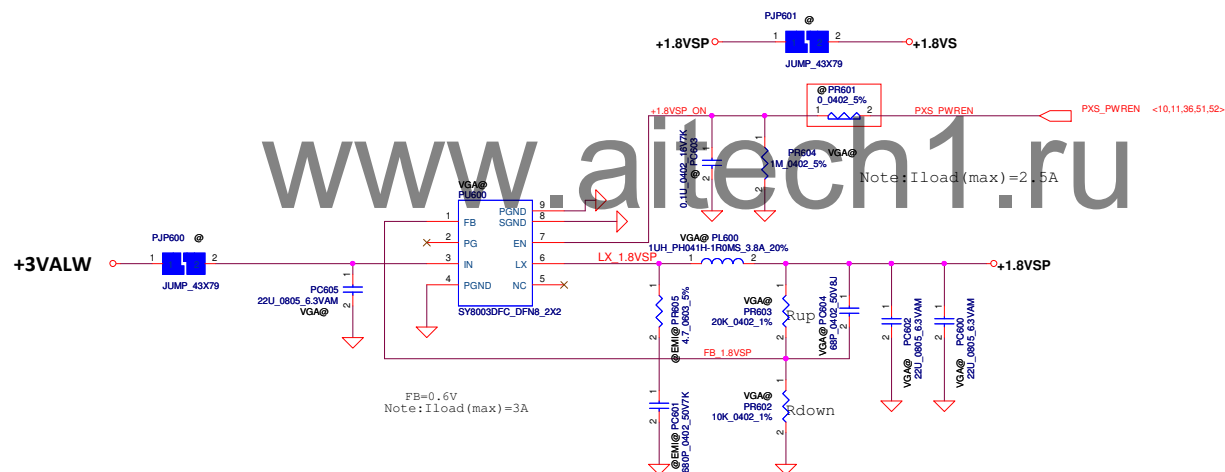
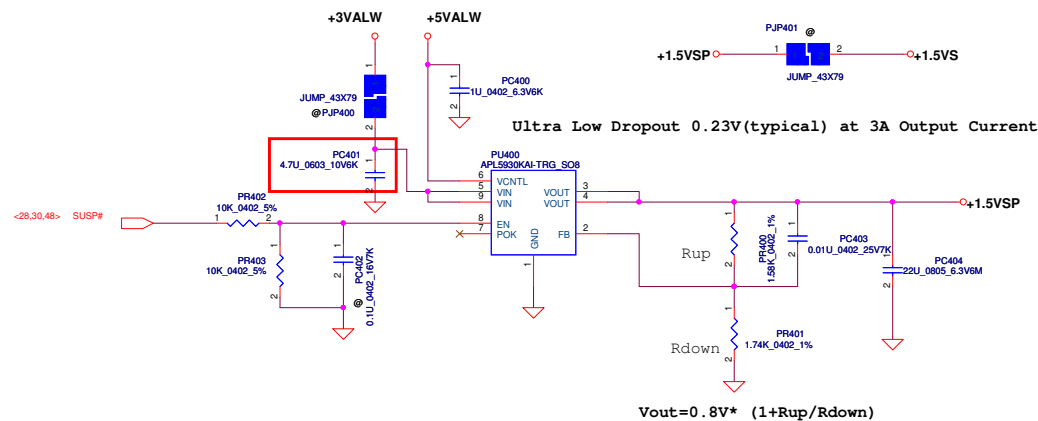




3VALWP
 TDC 5.95A
 Peak Current 8.5A
 OCP current 10.2A
 TYP MAX
 H/S Rds(on) : 22mohm , 30mohm
 L/S Rds(on) : 10.8mohm , 13.6mohm



5VALWP
 TDC 5.96A
 Peak Current 8.51A
 OCP current 10.2A
 TYP MAX
 H/S Rds(on) : 22mohm , 30mohm
 L/S Rds(on) : 10.8mohm , 13.6mohm



TDC=9A
Peak Current=13A
OCP=16A

<10,11,36,47,52> PXS_PWREN

@PR1103
0_0402_5%

@PC1104
0.1U_0402_16V7K

PR1105 VGA@
470K_0402_1%

+3VS

PR1110
100K_0402_5%

PR1102 VGA@
154K_0402_1%

EN +1.35VGPUP

FB +1.35VGPUP

RF +1.35VGPUP

PR1107 VGA@
9.09K_0402_1%

PR1108 VGA@
10K_0402_1%

PU1100 VGA@

PGOOD VBST

TRIP

EN

VFB

TST

TP

TPS51212DSCR_SON10_3X3

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VGA@
PR1101
2.2_0603_5%

VGA@
PC1103
0.1U_0603_25V7K

BST +1.35VGPUP

UG +1.35VGPUP

SW +1.35VGPUP

LG +1.35VGPUP

VGA@
PC1105
1U_0603_10V6K

VGA@
PQ1101
AON7752

VGA@
PQ1101
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+1.35VGPUP_B+

@EM1
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@EM1
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VGA@_EMI@ PL1100
FBM4516HS720NT_2P

B+

+1.35VGPUP

@PJP1100
JUMP_43X118
@PJP1101
JUMP_43X118

+1.35VS_VGA

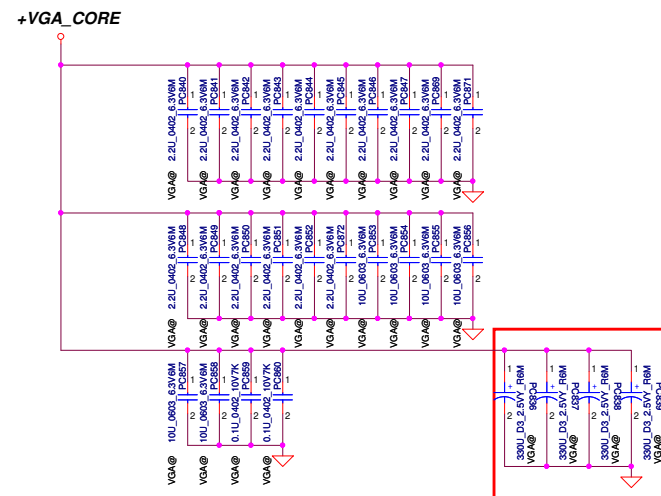
+1.35VGPUP

VGA@
PC1108
330U_25V_M

ESR=16m ohm

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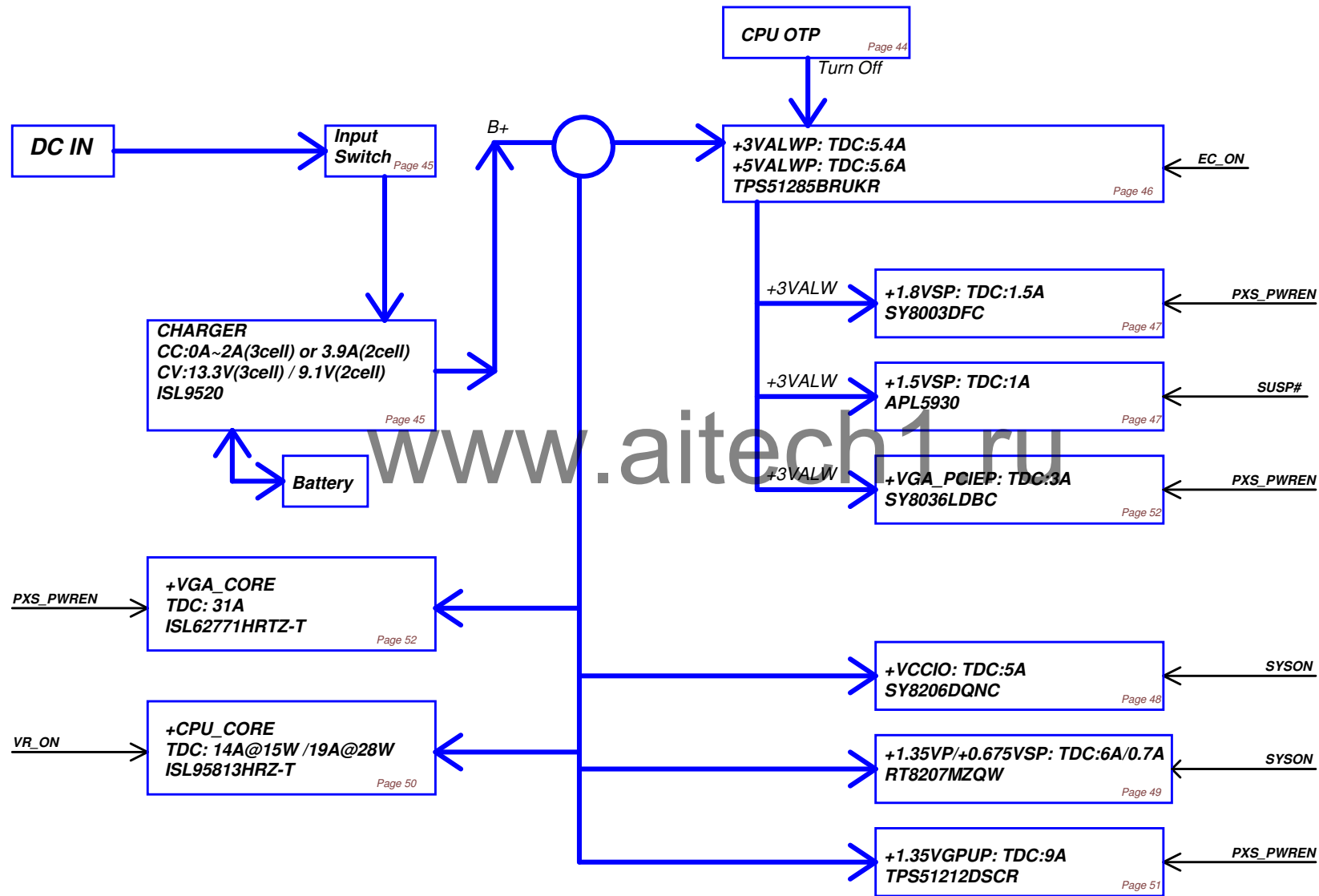
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/01/20		Deciphered Date		2015/01/19		Title	
										PWR +1.35VGPU	
										Size	
										Document Number	
										LA-B012P	
										Date	
										Tuesday, August 05, 2014	
										Sheet	
										51 of 55	
										Rev	
										1.0	



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Power block



Page 1

change PR535(28W@) from 432 to 20
change PR507(28W@) from 113K to 2
change PR551 from 2.8K to 5.23K
add PC522 82pF
add PR533 0-ohm

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Date:		Tuesday, August 05, 2014		Sheet 55 of 55		Document Number LA-B012P